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ATX
Ver: 1.0

Basinfall Platform

CPU:

Skylake X/Kabylake X

System Chipset:

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel I219+I211

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)*

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

*PCI Express (X16) Slot * 2*

*PCI Express (X8) Slot * 1*

*PCI Express (X4) Slot * 1*

*PCI Express (X1) Slot * 2*

Other:

*SATA3.0 *8*

*USB2.0 *6 Ports (2R/4F)*

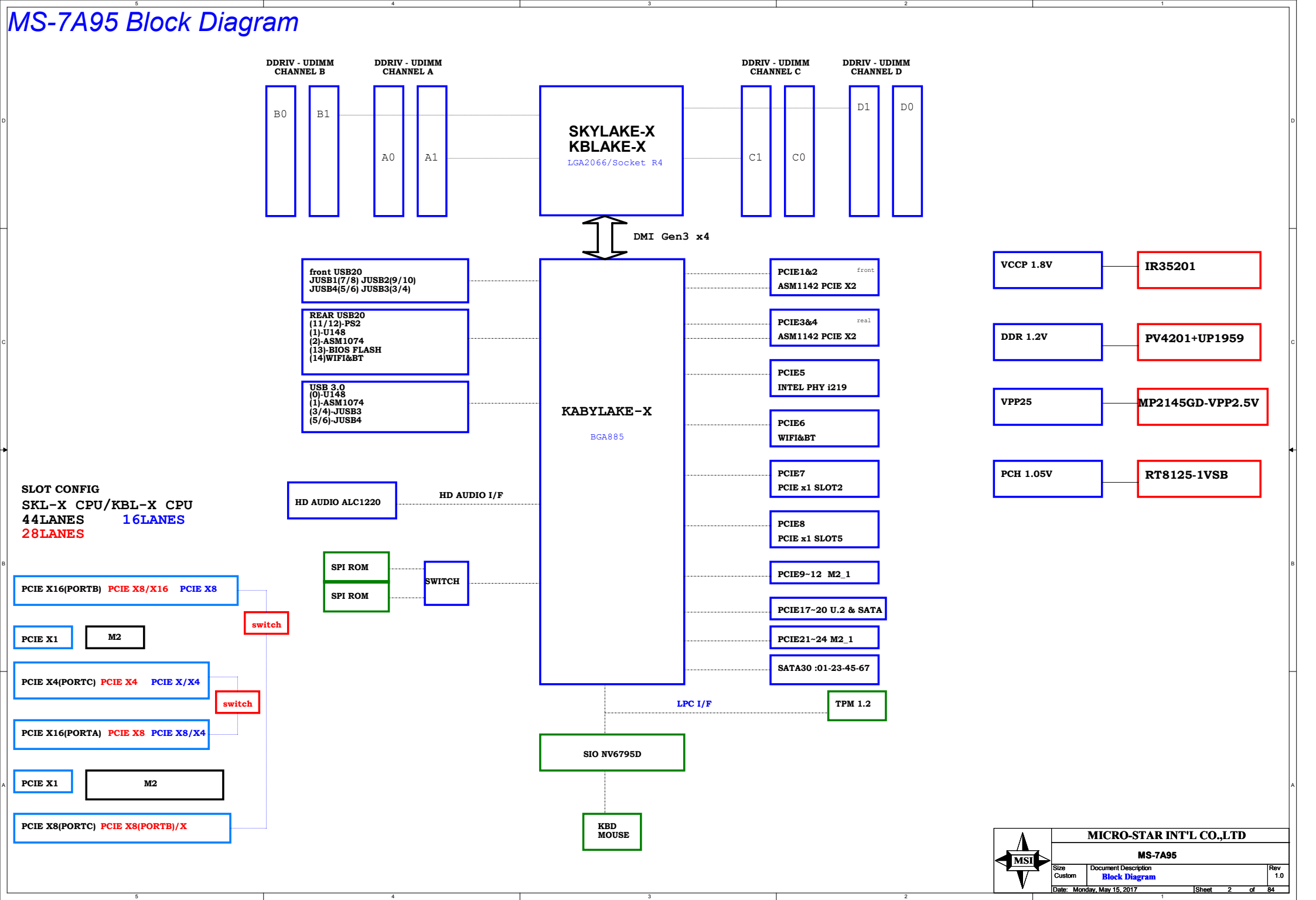
*REAR USB30*5 + USB3.1*1 & TYPEC*1*

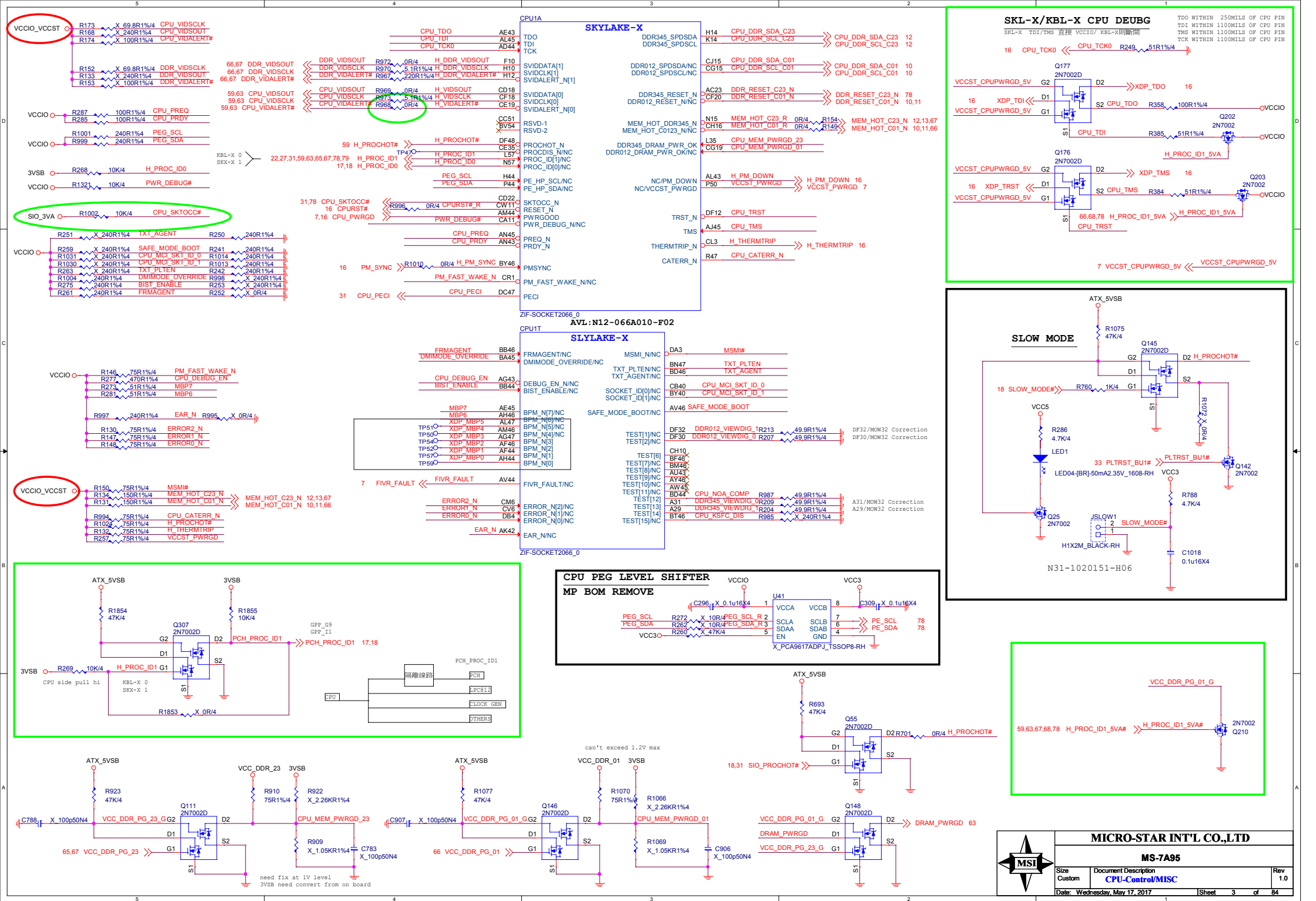
*FRONT USB3.0 *4+TYPEC*1*



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MS-7A95 Block Diagram





MEM_MA_DATA[63.0] <>> MEM_MA_DATA[63.0] 10

CPU1B		SKYLAKE-X	
MEM_MA_DATA63	DD52	DDR0_DQ[63]/NC	DD18
MEM_MA_DATA62	DE1	DDR0_DQS_DP17/NC	DD19
MEM_MA_DATA61	DE48	DDR0_DQS_DN17/NC	DD50
MEM_MA_DATA60	DE49	DDR0_DQS_DP16/NC	DF50
MEM_MA_DATA59	DA51	DDR0_DQS_DN16/NC	CU47
MEM_MA_DATA58	DE52	DDR0_DQS_DP15/NC	CU47
MEM_MA_DATA57	DE49	DDR0_DQS_DN15/NC	DD44
MEM_MA_DATA56	DE49	DDR0_DQS_DP14/NC	DF44
MEM_MA_DATA55	CP48	DDR0_DQS_DN14/NC	DD38
MEM_MA_DATA54	CV48	DDR0_DQS_DP13/NC	DF38
MEM_MA_DATA53	CP48	DDR0_DQS_DN13/NC	CV14
MEM_MA_DATA52	CP48	DDR0_DQS_DP12/NC	DE14
MEM_MA_DATA51	CR49	DDR0_DQS_DN12/NC	CV8
MEM_MA_DATA50	CU49	DDR0_DQS_DP11/NC	DB8
MEM_MA_DATA49	CV48	DDR0_DQS_DN11/NC	CR3
MEM_MA_DATA48	CU45	DDR0_DQS_DP10/NC	CP2
MEM_MA_DATA47	DD46	DDR0_DQS_DN10/NC	CB4
MEM_MA_DATA46	DE45	DDR0_DQS_DP9/NC	CD4
MEM_MA_DATA45	DB42	DDR0_DQS_DN9/NC	DE20
MEM_MA_DATA44	DD42	DDR0_DQS_DP8/NC	DA21
MEM_MA_DATA43	DA45	DDR0_DQS_DN8/NC	CV50
MEM_MA_DATA42	DB46	DDR0_DQS_DP7/NC	DB50
MEM_MA_DATA41	DE43	DDR0_DQS_DN7/NC	CR47
MEM_MA_DATA40	CP45	DDR0_DQS_DP6/NC	CU47
MEM_MA_DATA39	DD43	DDR0_DQS_DN6/NC	CV44
MEM_MA_DATA38	DE39	DDR0_DQS_DP5/NC	DB44
MEM_MA_DATA37	DD36	DDR0_DQS_DN5/NC	DB38
MEM_MA_DATA36	DB36	DDR0_DQS_DP4/NC	CV38
MEM_MA_DATA35	DE36	DDR0_DQS_DN4/NC	DD14
MEM_MA_DATA34	DD40	DDR0_DQS_DP3/NC	DF14
MEM_MA_DATA33	DE37	DDR0_DQS_DN3/NC	DF8
MEM_MA_DATA32	DA37	DDR0_DQS_DP2/NC	DD8
MEM_MA_DATA31	DA15	DDR0_DQS_DN2/NC	CU5
MEM_MA_DATA30	DE15	DDR0_DQS_DP1/NC	CT4
MEM_MA_DATA29	DB12	DDR0_DQS_DN1/NC	CH4
MEM_MA_DATA28	DA13	DDR0_DQS_DP0/NC	CF4
MEM_MA_DATA27	DD18		
MEM_MA_DATA26	DE16		
MEM_MA_DATA25	DE13		
MEM_MA_DATA24	DD12		
MEM_MA_DATA23	DE9		
MEM_MA_DATA22	DA9		
MEM_MA_DATA21	DD8		
MEM_MA_DATA20	DB6		
MEM_MA_DATA19	DD10		
MEM_MA_DATA18	DB10		
MEM_MA_DATA17	DE10		
MEM_MA_DATA16	DA7		
MEM_MA_DATA15	CV2		
MEM_MA_DATA14	CT2		
MEM_MA_DATA13	CN5		
MEM_MA_DATA12	CM4		
MEM_MA_DATA11	CV3		
MEM_MA_DATA10	CV4		
MEM_MA_DATA9	CN3		
MEM_MA_DATA8	CR5		
MEM_MA_DATA7	CJ3		
MEM_MA_DATA6	CG3		
MEM_MA_DATA5	CC5		
MEM_MA_DATA4	CA5		
MEM_MA_DATA3	CJ5		
MEM_MA_DATA2	CG5		
MEM_MA_DATA1	CC3		
MEM_MA_DATA0	CA3		
DE19	DDR0_ECC[7]/NC	DDR0_ODT[3]/NC	DE33
DE21	DDR0_ECC[6]/NC	DDR0_ODT[2]/NC	DB32
DE18	DDR0_ECC[5]/NC	DDR0_ODT[1]/NC	CU31
DE19	DDR0_ECC[4]/NC	DDR0_ODT[0]/NC	CU31
DE21	DDR0_ECC[3]/NC		
CV20	DDR0_ECC[2]/NC		
CV19	DDR0_ECC[1]/NC		
MEM_MA_CLK_H3	MEM_MA_CLK_H3	MEM_MA_CLK_H3	MEM_MA_CLK_H3
MEM_MA_CLK_L3	MEM_MA_CLK_L3	MEM_MA_CLK_L3	MEM_MA_CLK_L3
MEM_MA_CLK_H2	MEM_MA_CLK_H2	MEM_MA_CLK_H2	MEM_MA_CLK_H2
MEM_MA_CLK_L2	MEM_MA_CLK_L2	MEM_MA_CLK_L2	MEM_MA_CLK_L2
MEM_MA_CLK_H1	MEM_MA_CLK_H1	MEM_MA_CLK_H1	MEM_MA_CLK_H1
MEM_MA_CLK_L1	MEM_MA_CLK_L1	MEM_MA_CLK_L1	MEM_MA_CLK_L1
MEM_MA_CLK_H0	MEM_MA_CLK_H0	MEM_MA_CLK_H0	MEM_MA_CLK_H0
MEM_MA_CLK_L0	MEM_MA_CLK_L0	MEM_MA_CLK_L0	MEM_MA_CLK_L0
MEM_MA_BG_1	MEM_MA_BG_1	MEM_MA_BG_1	MEM_MA_BG_1
MEM_MA_BG_0	MEM_MA_BG_0	MEM_MA_BG_0	MEM_MA_BG_0
MEM_MA_BA_1	MEM_MA_BA_1	MEM_MA_BA_1	MEM_MA_BA_1
MEM_MA_BA_0	MEM_MA_BA_0	MEM_MA_BA_0	MEM_MA_BA_0

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MEM_MB_DATA[63.0] <>> MEM_MB_DATA[63.0] 11

CPU1C		SKYLAKE-X	
MEM_MB_DATA63	CE49	DDR1_DQ[63]/NC	CP18
MEM_MB_DATA62	CL49	DDR1_DQS_DP17/NC	CT18
MEM_MB_DATA61	CL49	DDR1_DQS_DN17/NC	CU49
MEM_MB_DATA60	CM50	DDR1_DQS_DP16/NC	CK48
MEM_MB_DATA59	CF48	DDR1_DQS_DN16/NC	CK44
MEM_MB_DATA58	CH48	DDR1_DQS_DP15/NC	CU44
MEM_MB_DATA57	CE51	DDR1_DQS_DN15/NC	CK44
MEM_MB_DATA56	CL51	DDR1_DQS_DP14/NC	CU41
MEM_MB_DATA55	CK46	DDR1_DQS_DN14/NC	CK38
MEM_MB_DATA54	CL45	DDR1_DQS_DP13/NC	CU38
MEM_MB_DATA53	CH43	DDR1_DQS_DN13/NC	CU34
MEM_MB_DATA52	CH42	DDR1_DQS_DP12/NC	CU34
MEM_MB_DATA51	CG45	DDR1_DQS_DN12/NC	CU34
MEM_MB_DATA50	CH46	DDR1_DQS_DP11/NC	CU34
MEM_MB_DATA49	CL43	DDR1_DQS_DN11/NC	CU34
MEM_MB_DATA48	CK43	DDR1_DQS_DP10/NC	CU34
MEM_MB_DATA47	CU43	DDR1_DQS_DN10/NC	CU34
MEM_MB_DATA46	CV42	DDR1_DQS_DP9/NC	CU34
MEM_MB_DATA45	CP40	DDR1_DQS_DN9/NC	CU34
MEM_MB_DATA44	CH39	DDR1_DQS_DP8/NC	CU34
MEM_MB_DATA43	CR43	DDR1_DQS_DN8/NC	CU34
MEM_MB_DATA42	CP42	DDR1_DQS_DP7/NC	CU34
MEM_MB_DATA41	CV40	DDR1_DQS_DN7/NC	CU34
MEM_MB_DATA40	CU39	DDR1_DQS_DP6/NC	CU34
MEM_MB_DATA39	CK40	DDR1_DQS_DN6/NC	CU34
MEM_MB_DATA38	CL37	DDR1_DQS_DP5/NC	CU34
MEM_MB_DATA37	CG37	DDR1_DQS_DN5/NC	CU34
MEM_MB_DATA36	CH36	DDR1_DQS_DP4/NC	CU34
MEM_MB_DATA35	CH40	DDR1_DQS_DN4/NC	CU34
MEM_MB_DATA34	CG39	DDR1_DQS_DP3/NC	CU34
MEM_MB_DATA33	CL36	DDR1_DQS_DN3/NC	CU34
MEM_MB_DATA32	CK36	DDR1_DQS_DP2/NC	CU34
MEM_MB_DATA31	CU36	DDR1_DQS_DN2/NC	CU34
MEM_MB_DATA30	CE15	DDR1_DQS_DP1/NC	CU34
MEM_MB_DATA29	CA13	DDR1_DQS_DN1/NC	CU34
MEM_MB_DATA28	CB12	DDR1_DQS_DP0/NC	CU34
MEM_MB_DATA27	CB16		
MEM_MB_DATA26	CA15		
MEM_MB_DATA25	CE13		
MEM_MB_DATA24	CU12		
MEM_MB_DATA23	CT14		
MEM_MB_DATA22	CR13		
MEM_MB_DATA21	CK14		
MEM_MB_DATA20	CJ13		
MEM_MB_DATA19	CR15		
MEM_MB_DATA18	CN15		
MEM_MB_DATA17	CM15		
MEM_MB_DATA16	CK12		
MEM_MB_DATA15	CP10		
MEM_MB_DATA14	CR9		
MEM_MB_DATA13	CU7		
MEM_MB_DATA12	CJ7		
MEM_MB_DATA11	CM10		
MEM_MB_DATA10	CL9		
MEM_MB_DATA9	CU7		
MEM_MB_DATA8	CR7		
MEM_MB_DATA7	CG9		
MEM_MB_DATA6	CF8		
MEM_MB_DATA5	BY8		
MEM_MB_DATA4	CA9		
MEM_MB_DATA3	CF10		
MEM_MB_DATA2	CU10		
MEM_MB_DATA1	CC7		
MEM_MB_DATA0	CA7		
MEM_MB_CLK_H3	MEM_MB_CLK_H3	MEM_MB_CLK_H3	MEM_MB_CLK_H3
MEM_MB_CLK_L3	MEM_MB_CLK_L3	MEM_MB_CLK_L3	MEM_MB_CLK_L3
MEM_MB_CLK_H2	MEM_MB_CLK_H2	MEM_MB_CLK_H2	MEM_MB_CLK_H2
MEM_MB_CLK_L2	MEM_MB_CLK_L2	MEM_MB_CLK_L2	MEM_MB_CLK_L2
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MEM_MB_CLK_L0	MEM_MB_CLK_L0	MEM_MB_CLK_L0	MEM_MB_CLK_L0
MEM_MB_BG_1	MEM_MB_BG_1	MEM_MB_BG_1	MEM_MB_BG_1
MEM_MB_BG_0	MEM_MB_BG_0	MEM_MB_BG_0	MEM_MB_BG_0
MEM_MB_BA_1	MEM_MB_BA_1	MEM_MB_BA_1	MEM_MB_BA_1
MEM_MB_BA_0	MEM_MB_BA_0	MEM_MB_BA_0	MEM_MB_BA_0

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MEM_MB_DATA[63.0] <>> MEM_MB_DATA[63.0] 11

CPU1C		SKYLAKE-X	
MEM_MB_DATA63	CE49	DDR1_DQ[63]/NC	CP18
MEM_MB_DATA62	CL49	DDR1_DQS_DP17/NC	CT18
MEM_MB_DATA61	CL49	DDR1_DQS_DN17/NC	CU49
MEM_MB_DATA60	CM50	DDR1_DQS_DP16/NC	CK48
MEM_MB_DATA59	CF48	DDR1_DQS_DN16/NC	CK44
MEM_MB_DATA58	CH48	DDR1_DQS_DP15/NC	CU44
MEM_MB_DATA57	CE51	DDR1_DQS_DN15/NC	CK44
MEM_MB_DATA56	CL51	DDR1_DQS_DP14/NC	CU41
MEM_MB_DATA55	CK46	DDR1_DQS_DN14/NC	CK38
MEM_MB_DATA54	CL45	DDR1_DQS_DP13/NC	CU38
MEM_MB_DATA53	CH43	DDR1_DQS_DN13/NC	CU34
MEM_MB_DATA52	CH42	DDR1_DQS_DP12/NC	CU34
MEM_MB_DATA51	CG45	DDR1_DQS_DN12/NC	CU34
MEM_MB_DATA50	CH46	DDR1_DQS_DP11/NC	CU34
MEM_MB_DATA49	CL43	DDR1_DQS_DN11/NC	CU34
MEM_MB_DATA48	CK43	DDR1_DQS_DP10/NC	CU34
MEM_MB_DATA47	CU43	DDR1_DQS_DN10/NC	CU34
MEM_MB_DATA46	CV42	DDR1_DQS_DP9/NC	CU34
MEM_MB_DATA45	CP40	DDR1_DQS_DN9/NC	CU34
MEM_MB_DATA44	CH39	DDR1_DQS_DP8/NC	CU34
MEM_MB_DATA43	CR43	DDR1_DQS_DN8/NC	CU34
MEM_MB_DATA42	CP42	DDR1_DQS_DP7/NC	CU34
MEM_MB_DATA41	CV40	DDR1_DQS_DN7/NC	CU34
MEM_MB_DATA40	CU39	DDR1_DQS_DP6/NC	CU34
MEM_MB_DATA39	CK40	DDR1_DQS_DN6/NC	CU34
MEM_MB_DATA38	CL37	DDR1_DQS_DP5/NC	CU34
MEM_MB_DATA37	CG37	DDR1_DQS_DN5/NC	CU34
MEM_MB_DATA36	CH36	DDR1_DQS_DP4/NC	CU34
MEM_MB_DATA35	CH40	DDR1_DQS_DN4/NC	CU34
MEM_MB_DATA34	CG39	DDR1_DQS_DP3/NC	CU34
MEM_MB_DATA33	CL36	DDR1_DQS_DN3/NC	CU34
MEM_MB_DATA32	CK36	DDR1_DQS_DP2/NC	CU34
MEM_MB_DATA31	CU36	DDR1_DQS_DN2/NC	CU34
MEM_MB_DATA30	CE15	DDR1_DQS_DP1/NC	CU34
MEM_MB_DATA29	CA13	DDR1_DQS_DN1/NC	CU34
MEM_MB_DATA28	CB12	DDR1_DQS_DP0/NC	CU34
MEM_MB_DATA27	CB16		
MEM_MB_DATA26	CA15		
MEM_MB_DATA25	CE13		
MEM_MB_DATA24	CU12		
MEM_MB_DATA23	CT14		
MEM_MB_DATA22	CR13		
MEM_MB_DATA21	CK14		
MEM_MB_DATA20	CJ13		
MEM_MB_DATA19	CR15		
MEM_MB_DATA18	CN15		
MEM_MB_DATA17	CM15		
MEM_MB_DATA16	CK12		
MEM_MB_DATA15	CP10		
MEM_MB_DATA14	CR9		
MEM_MB_DATA13	CU7		
MEM_MB_DATA12	CJ7		
MEM_MB_DATA11	CM10		
MEM_MB_DATA10	CL9		
MEM_MB_DATA9	CU7		
MEM_MB_DATA8	CR7		
MEM_MB_DATA7	CG9		
MEM_MB_DATA6	CF8		
MEM_MB_DATA5	BY8		
MEM_MB_DATA4	CA9		
MEM_MB_DATA3	CF10		
MEM_MB_DATA2	CU10		
MEM_MB_DATA1	CC7		
MEM_MB_DATA0	CA7		
MEM_MB_CLK_H3	MEM_MB_CLK_H3	MEM_MB_CLK_H3	MEM_MB_CLK_H3
MEM_MB_CLK_L3	MEM_MB_CLK_L3	MEM_MB_CLK_L3	MEM_MB_CLK_L3
MEM_MB_CLK_H2	MEM_MB_CLK_H2	MEM_MB_CLK_H2	MEM_MB_CLK_H2
MEM_MB_CLK_L2	MEM_MB_CLK_L2	MEM_MB_CLK_L2	MEM_MB_CLK_L2
MEM_MB_CLK_H1	MEM_MB_CLK_H1	MEM_MB_CLK_H1	MEM_MB_CLK_H1
MEM_MB_CLK_L1	MEM_MB_CLK_L1	MEM_MB_CLK_L1	MEM_MB_CLK_L1
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MEM_MB_CLK_L0	MEM_MB_CLK_L0	MEM_MB_CLK_L0	MEM_MB_CLK_L0
MEM_MB_BG_1	MEM_MB_BG_1	MEM_MB_BG_1	MEM_MB_BG_1
MEM_MB_BG_0	MEM_MB_BG_0	MEM_MB_BG_0	MEM_MB_BG_0
MEM_MB_BA_1	MEM_MB_BA_1	MEM_MB_BA_1	MEM_MB_BA_1
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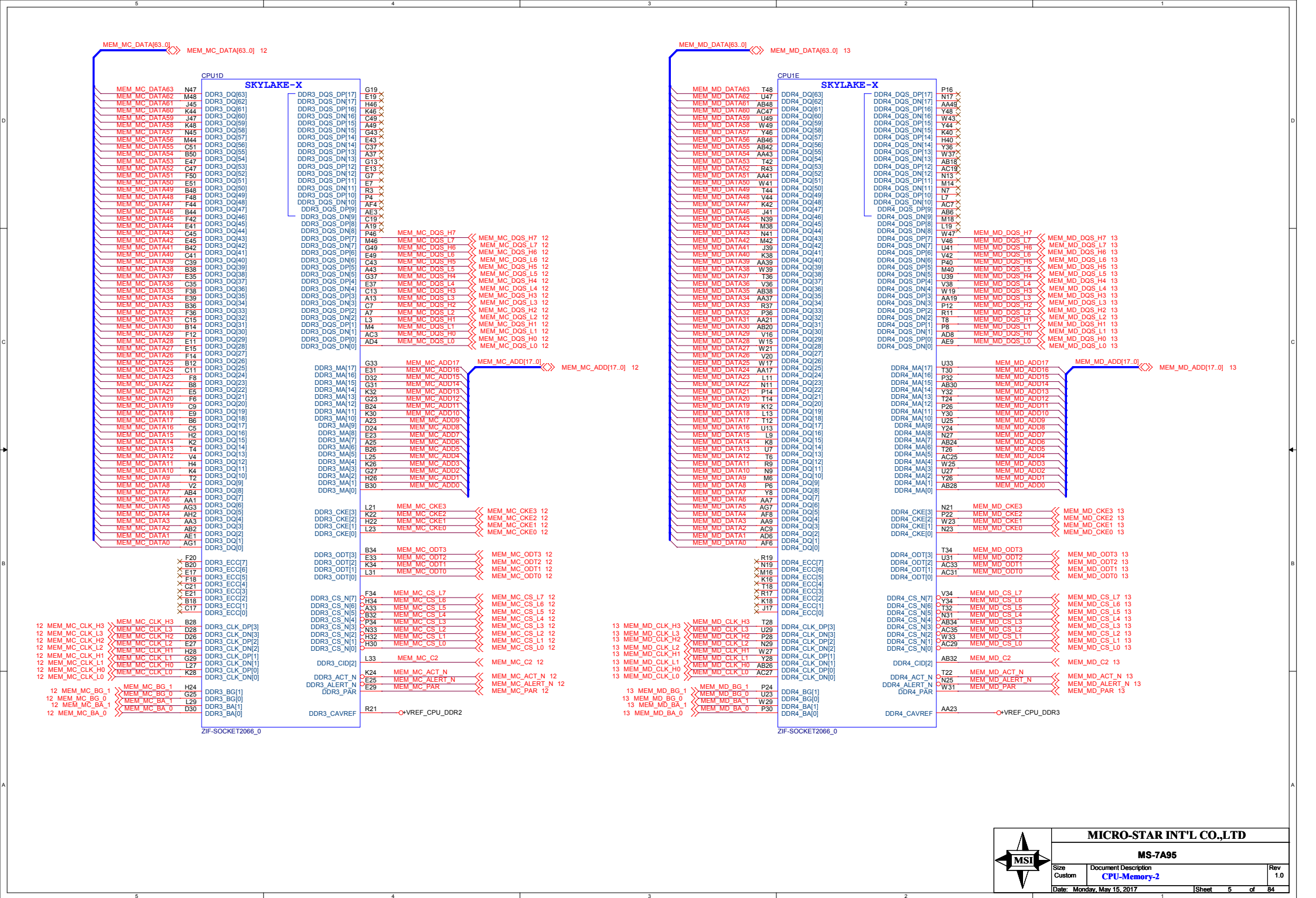
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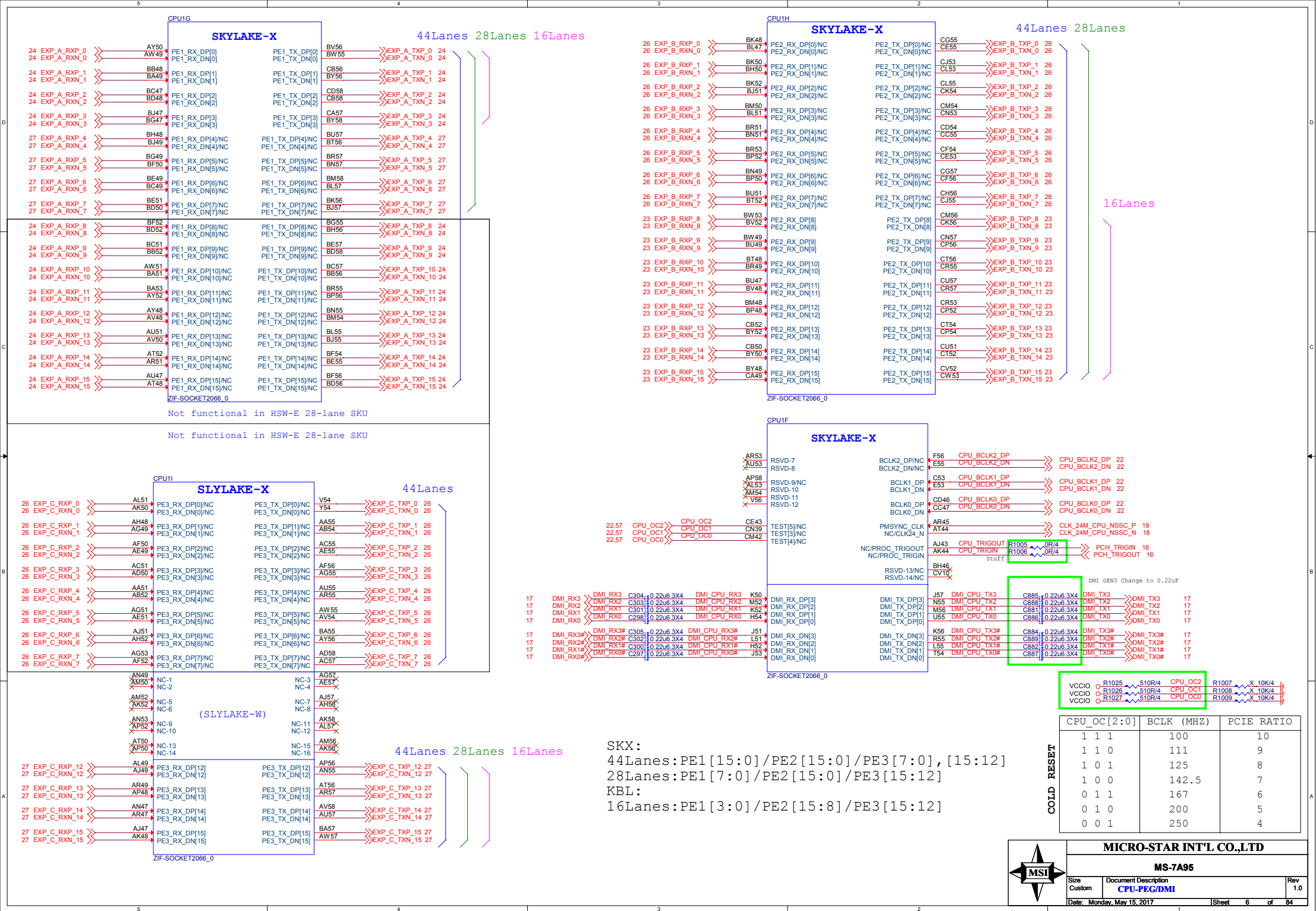


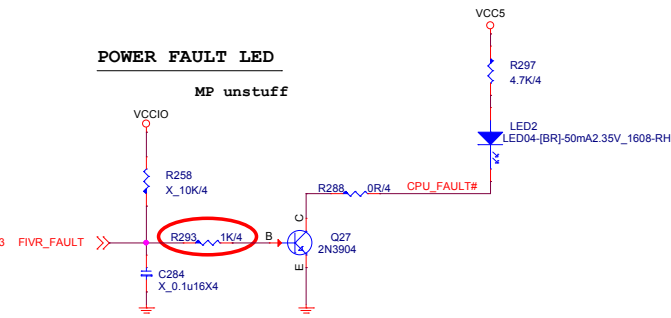
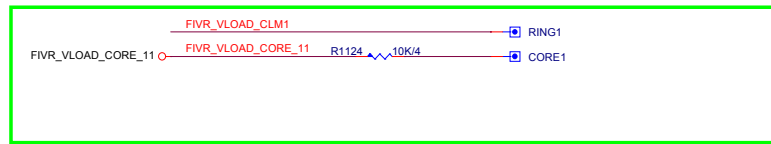
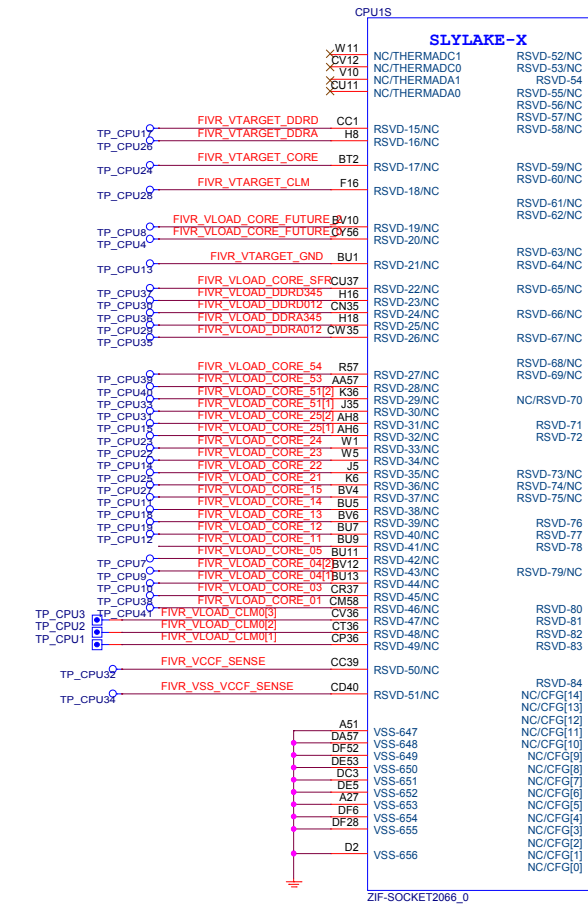
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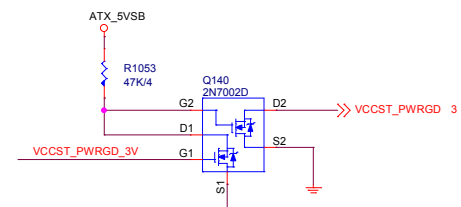
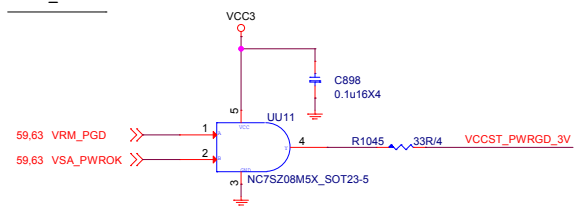
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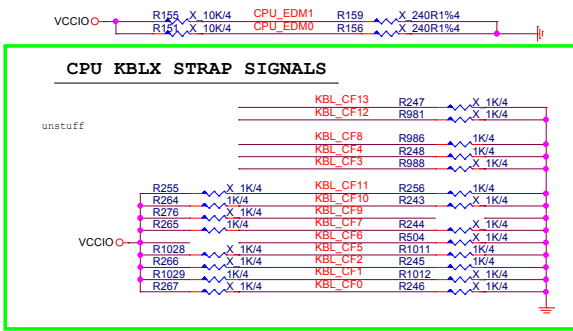
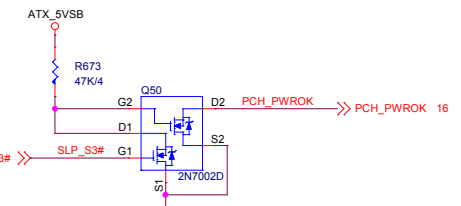
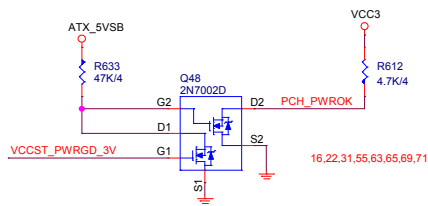




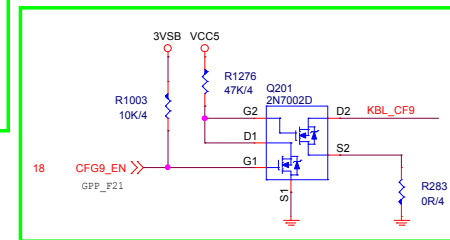
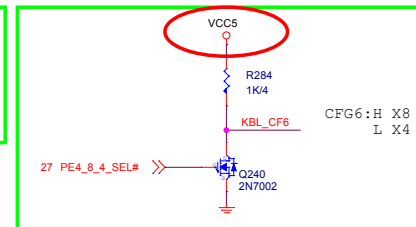
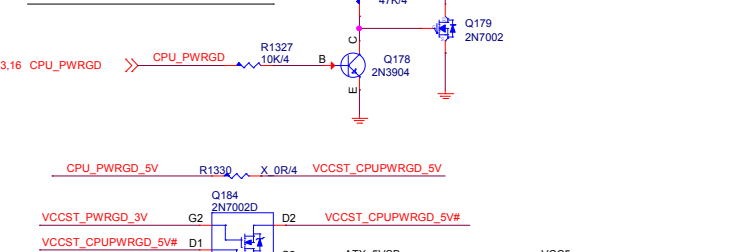
VCCST_PWRGD



PCH_PWROK



SKL-X/KBL-X CPU DEUBG



PCIE Strap

CFG6	CFG5	CFG2	PCIE
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0	0	1	1x8, 2x4
1	0	0	2x8
1	0	1	2x8
1	1	0	1x16
1	1	1	1x16

REVERSED

REVERSED

REVERSED

CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1	RSVD		
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVIO PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD

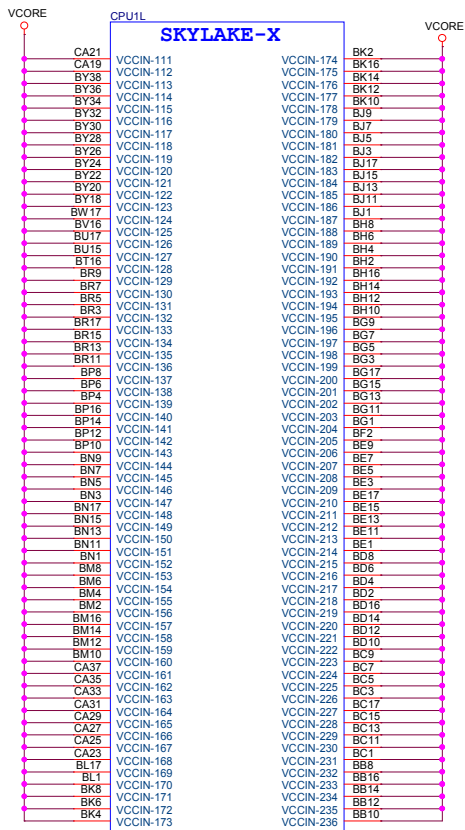
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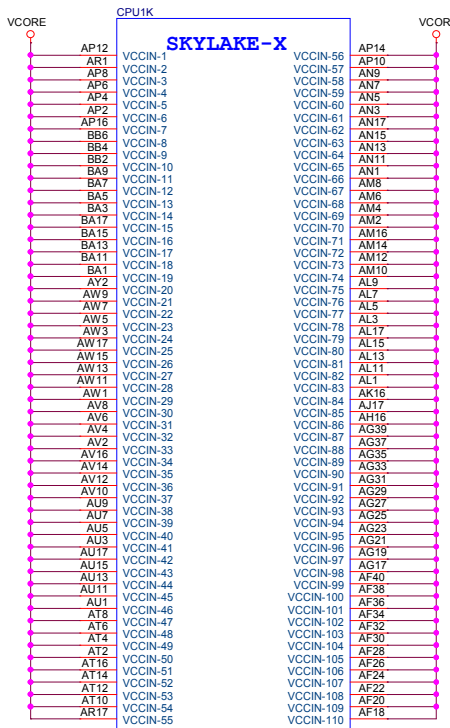
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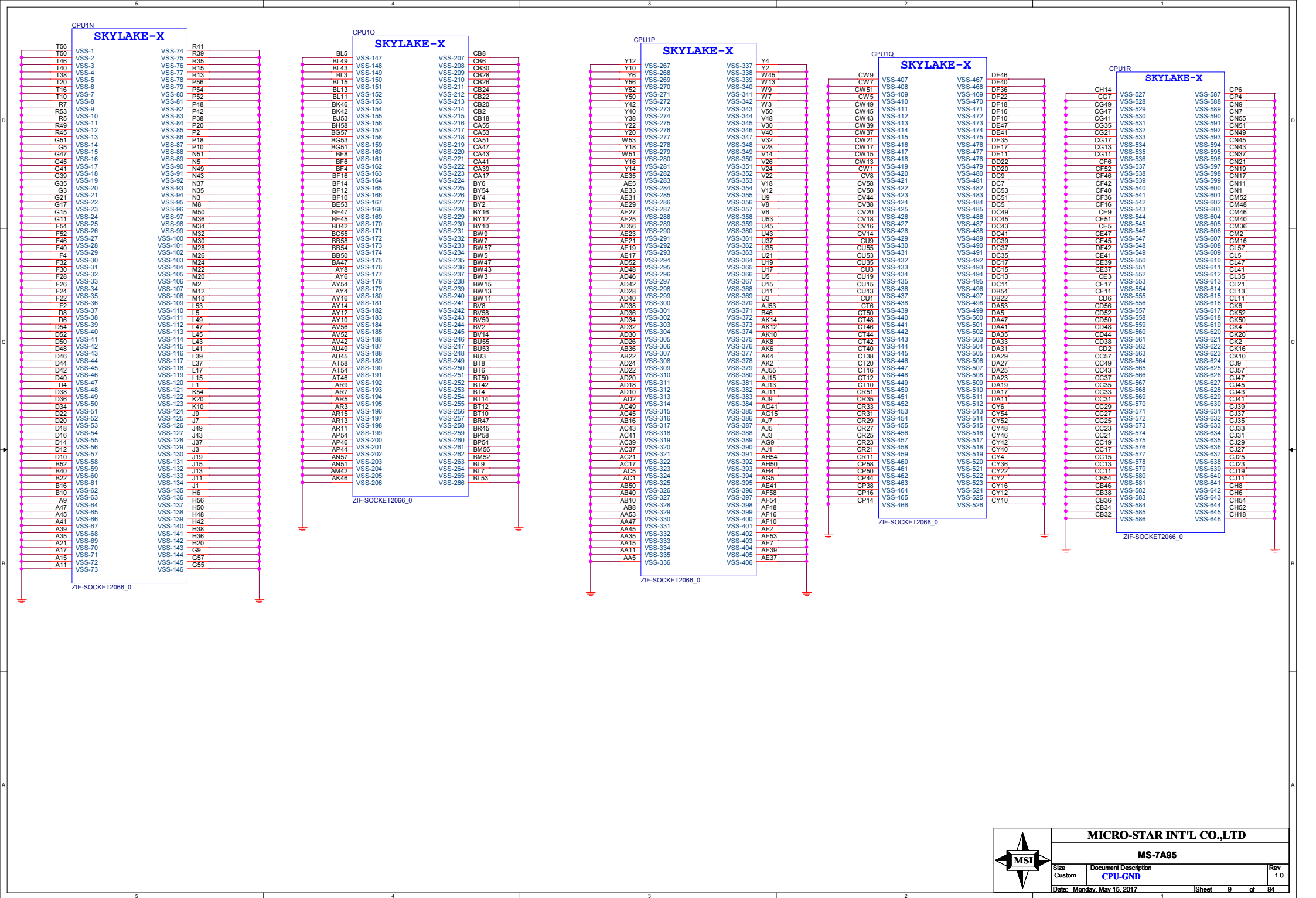
Size Custom Document Description **PCU-RSVD** Rev 1.0

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ZIF-SOCKET2066_0

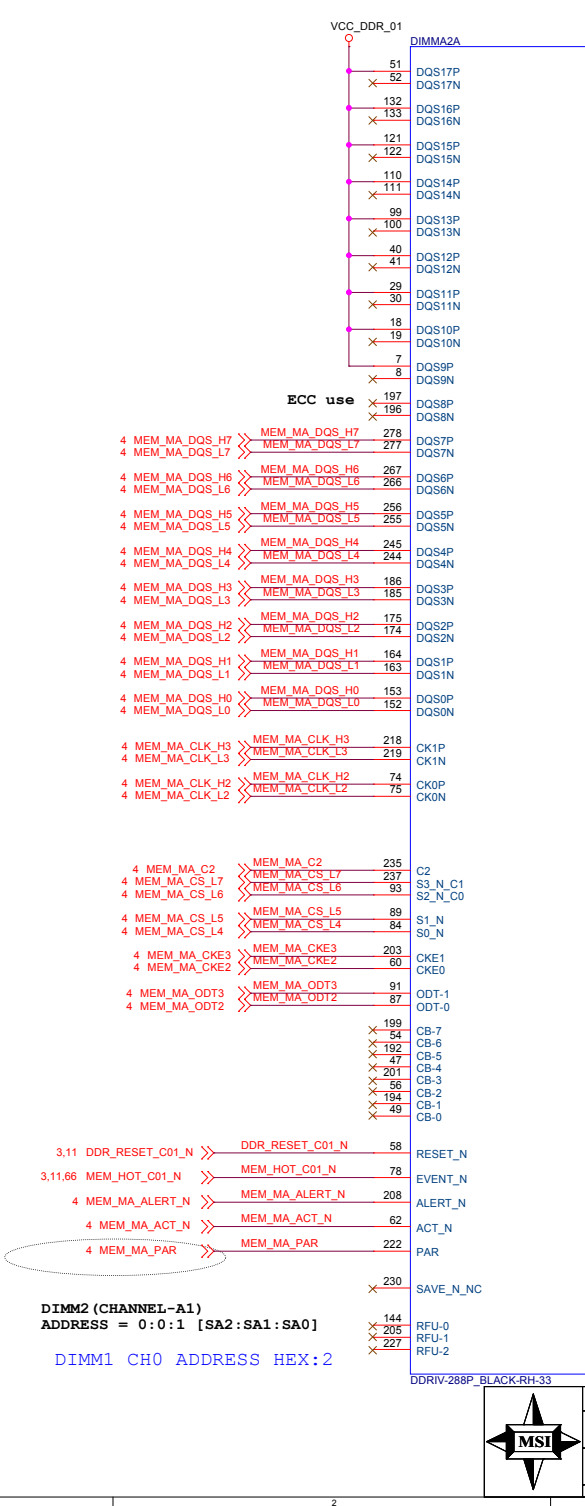




DDR IV DIMM1/2



DIMM1 (CHANNEL-A0)
ADDRESS = 0:0:0 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:0



DIMM2 (CHANNEL-A1)
ADDRESS = 0:0:1 [SA2:SA1:SA0]
DIMM1 CH0 ADDRESS HEX:2

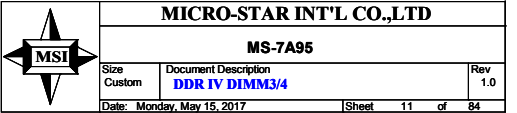
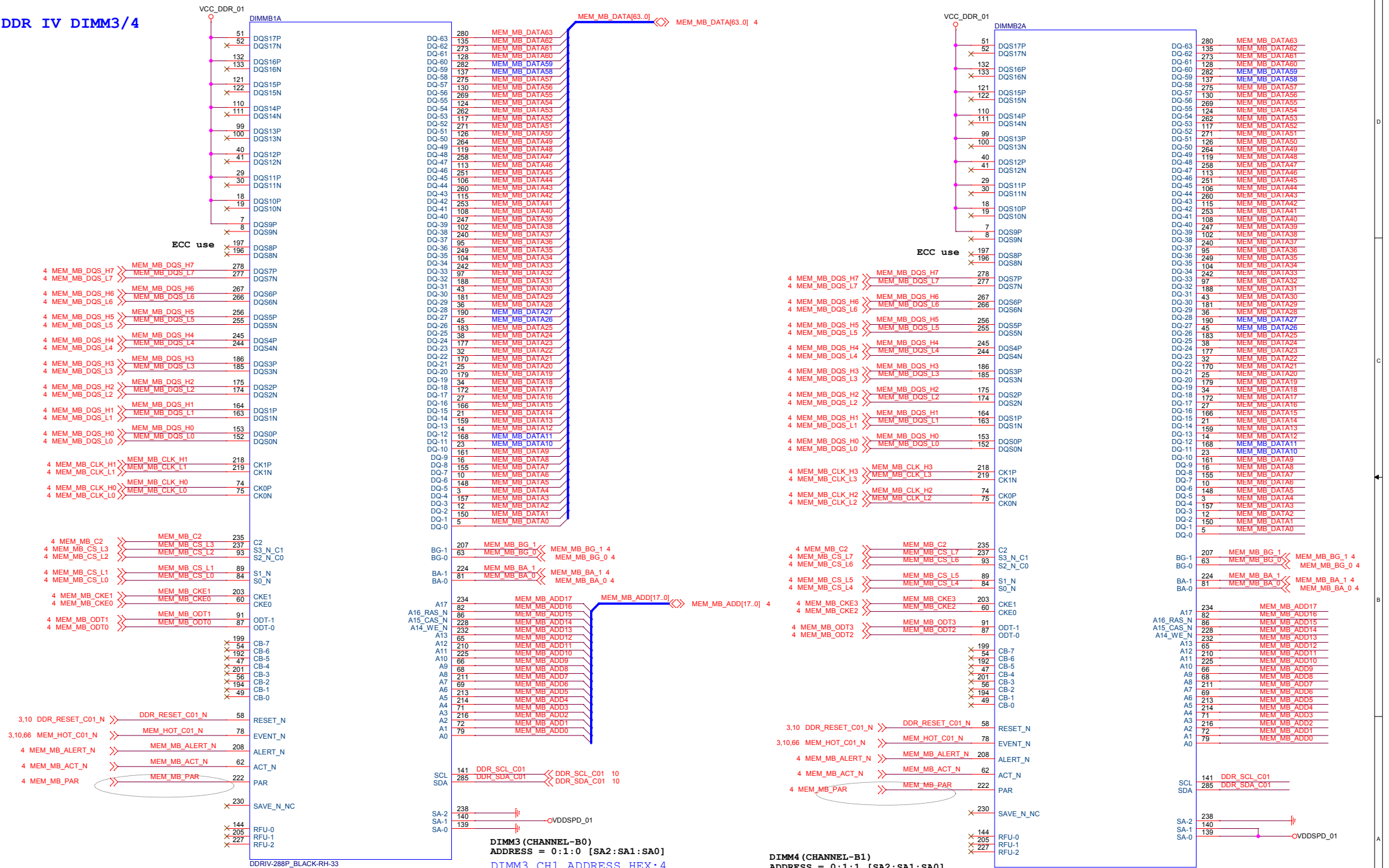
MICRO-STAR INT'L CO.,LTD

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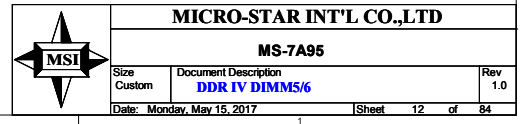
Size	Document Description	Rev
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DDR IV DIMM3/4

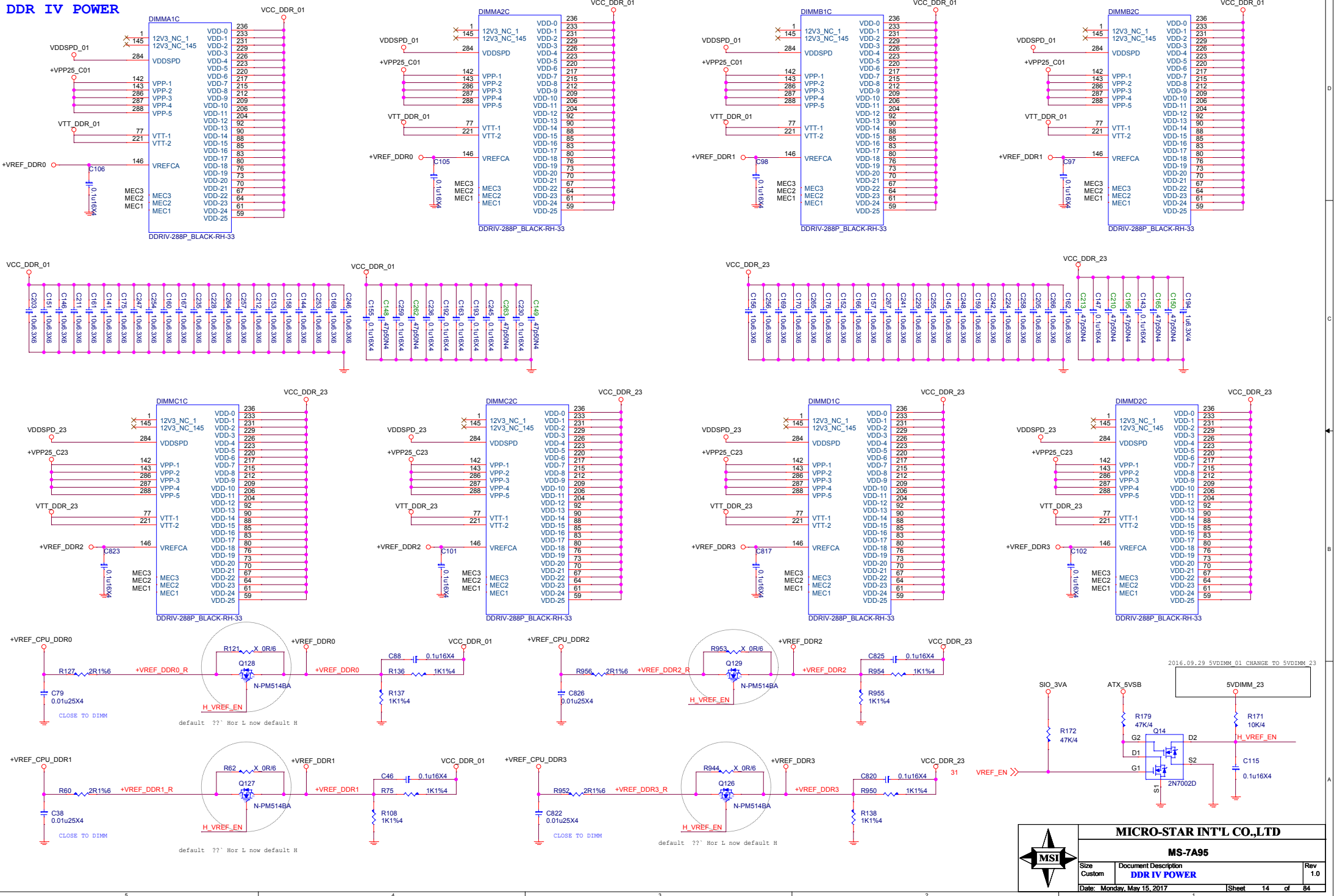


VCC_DDR_23

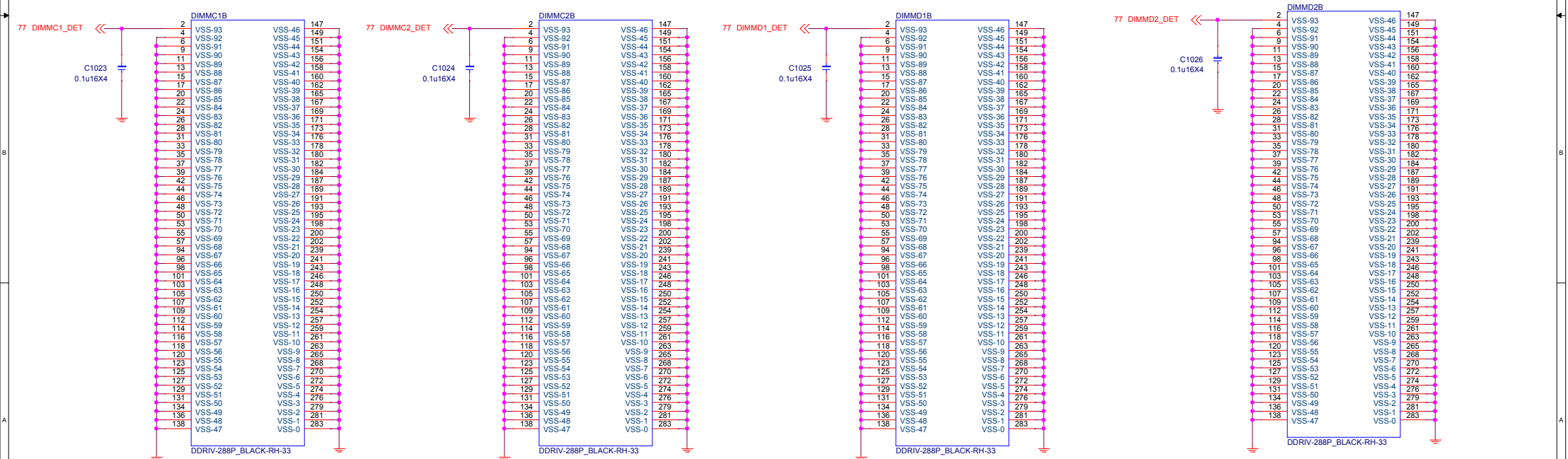
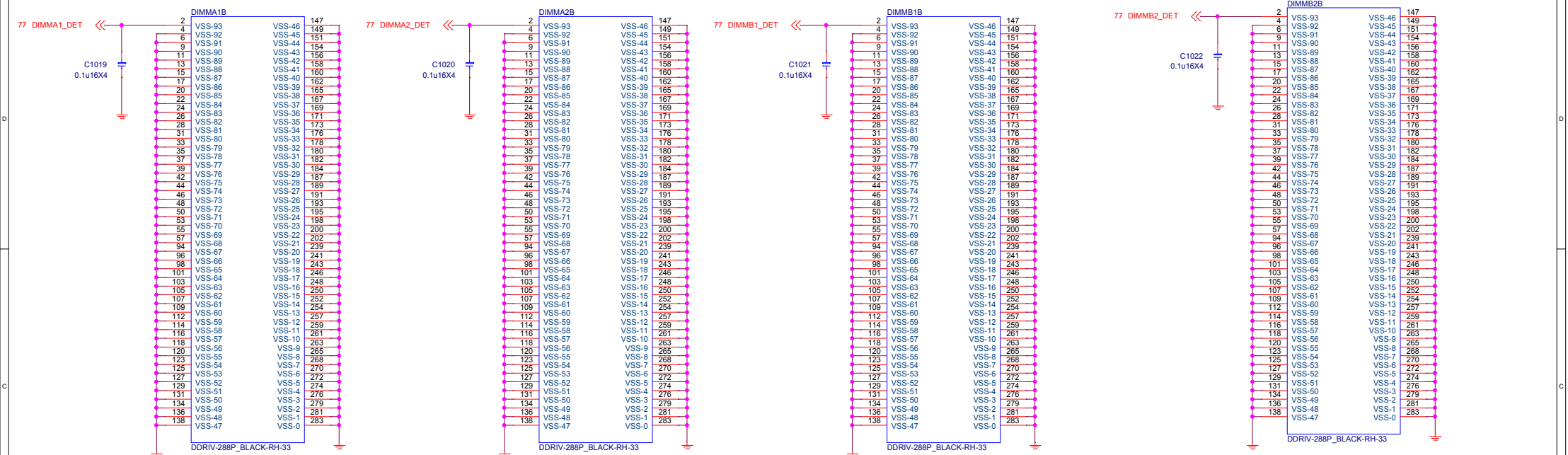


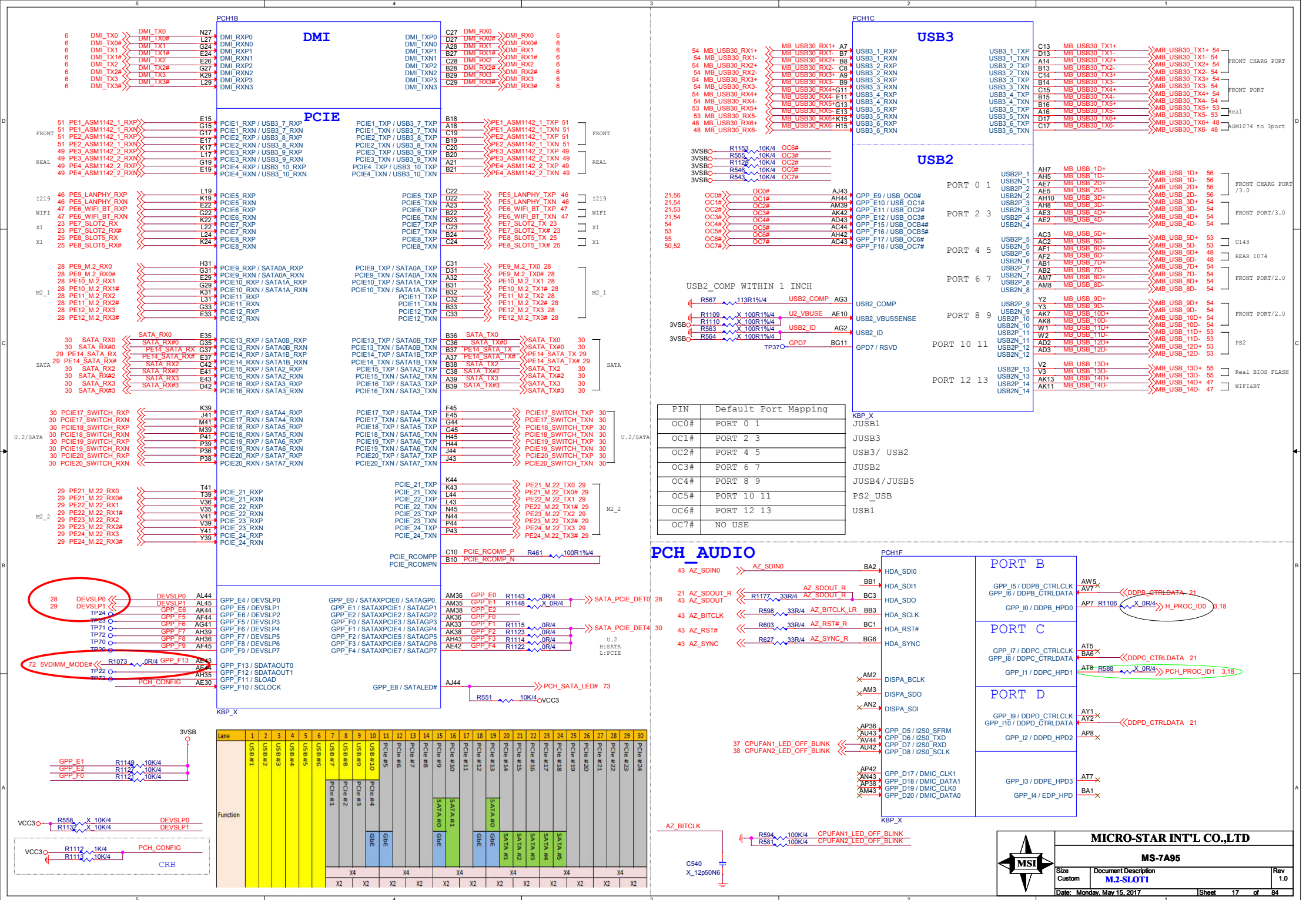


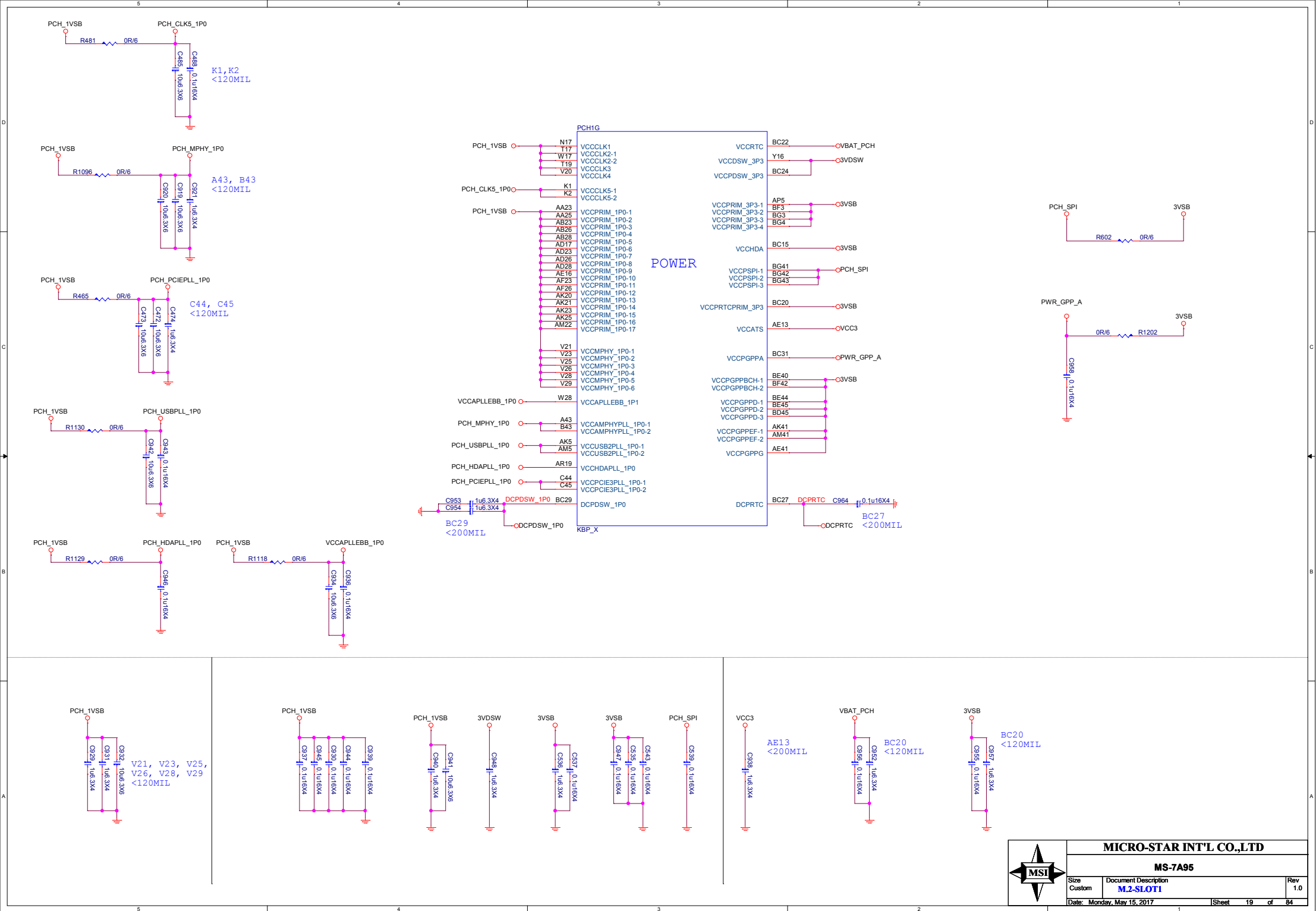
DDR IV POWER

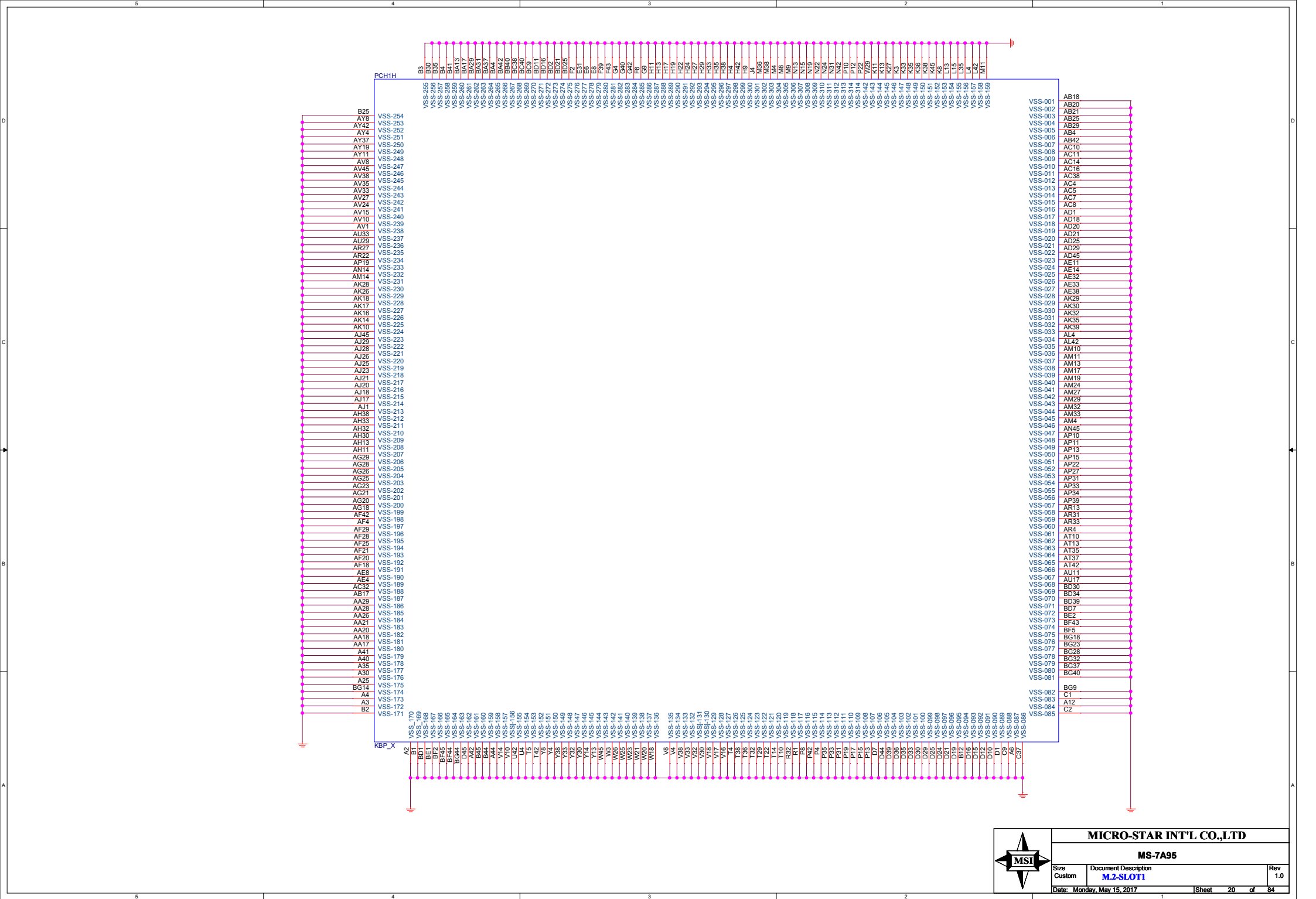



DDR IV GND











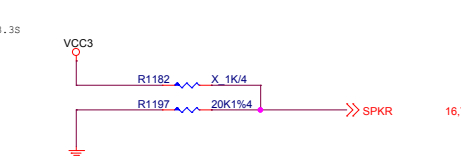
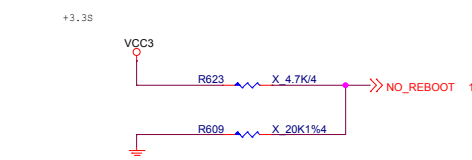
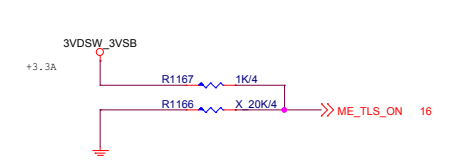
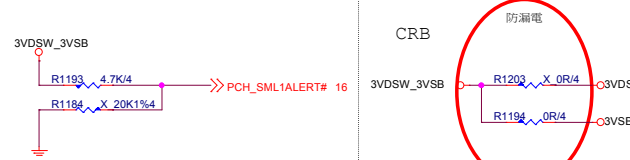
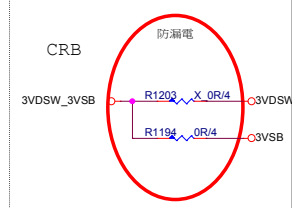
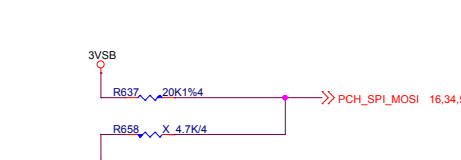
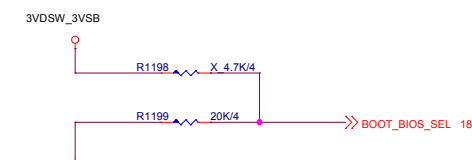
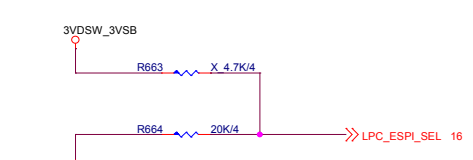
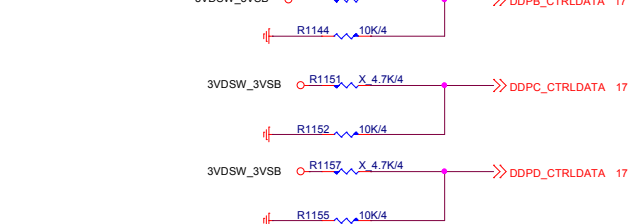
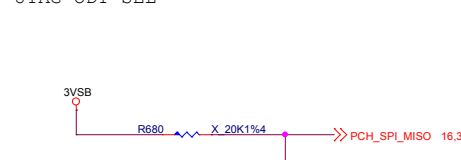
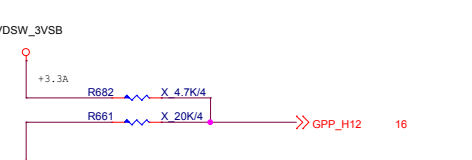
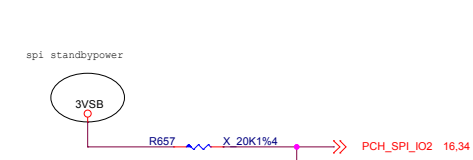
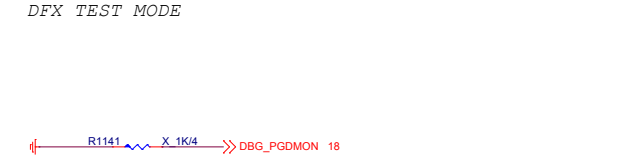
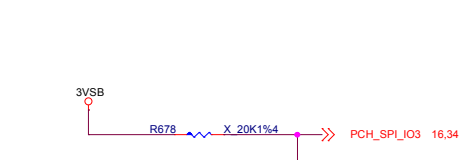
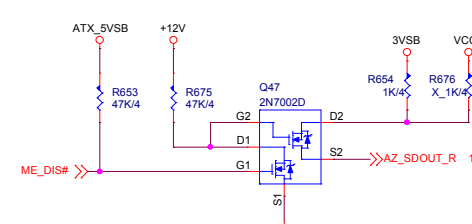
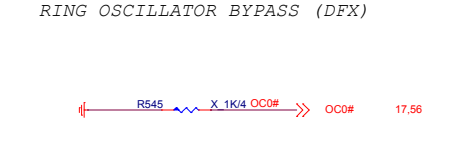
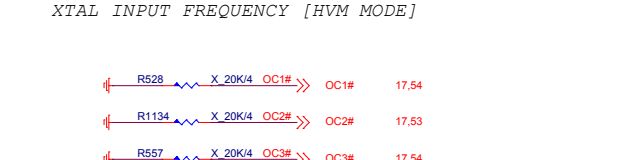



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<p><i>TOP SWAP OVERRIDE STRAP</i></p>  <p>HIGH: TOP_SWAP ENABLED LOW : TOP_SWAP DISABLED</p> <p>PCH HAS INTERNAL WEAK PD</p>	<p><i>No Reboot OPTION</i></p>  <p>0 : NO-REBOOT (Default) 1 : REBOOT</p> <p>PCH HAS INTERNAL WEAK PD</p>	<p><i>AMT and SBA with confidentiality</i></p>  <p>0 : DISABLE 1 : ENABLE (Default)</p>	<p><i>DCI ENABLE</i></p>  <p>0 : DCI DISABLE 1 : DCI ENABLE (Default)</p> <p>PCH HAS INTERNAL WEAK PD</p> 														
<p><i>Booot-HALT SEL STRAP</i></p>  <p>PCH HAS INTERNAL WEAK PU</p>	<p><i>Boot BIOS</i></p>  <p>0 : SPI 1 : LPC</p>	<p><i>LPC eSPI Mode</i></p>  <p>0 : LPC 1 : eSPI</p>	<p><i>DISPLAY PORT</i></p>  <p>0 : DISPLAY NOT DETECTED (Default) 1 : DISPLAY DETECTED</p>														
<p><i>JTAG ODT SEL</i></p>  <p>HIGH: JTAG ODT ENABLED LOW : JTAG ODT DISABLED</p> <p>PCH HAS INTERNAL WEAK PU</p>	<p><i>ESPI FLASH SHARING MODE</i></p>  <p>0 : MASTER ATTACHED FLASH SHARING 1 : SLAVE ATTACHED FLASH SHARING</p> <p>PCH HAS INTERNAL WEAK PD</p>	<p><i>CONSENT</i></p>  <p>0 : CONSENT STRAP ENABLE 1 : CONSENT STRAP ENABLE</p> <p>PCH HAS INTERNAL WEAK PU</p>	<p><i>DFX TEST MODE</i></p>  <p>UNSRUFF: NORMAL STUFF: TEST MODE</p>														
<p><i>PERSONALITY</i></p>  <p>HIGH: PERSONALITY ENABLED LOW : PERSONALITY DISABLED</p> <p>PCH HAS INTERNAL WEAK PU</p>	<p><i>HDA_SDO</i></p>  <p>0 : SECURITY MEASURES OVERRIDEN 1 : SECURITY PER FLASH DESCRIPTOR</p>	<p><i>RING OSCILLATOR BYPASS (DFX)</i></p>  <p>0 : Ring Oscillator bypass 1 : Normal Mode</p>	<p><i>XTAL INPUT FREQUENCY [HVM MODE]</i></p>  <table border="1"> <tr> <td rowspan="3">  </td> <td colspan="3">MICRO-STAR INT'L CO.,LTD</td> </tr> <tr> <td colspan="3">MS-7A95</td> </tr> <tr> <td>Size Custom</td> <td>Document Description PCH-Strap</td> <td>Rev 1.0</td> </tr> <tr> <td colspan="2">Date: Monday, May 15, 2017</td> <td>Sheet 21</td> <td>of 84</td> </tr> </table>		MICRO-STAR INT'L CO.,LTD			MS-7A95			Size Custom	Document Description PCH-Strap	Rev 1.0	Date: Monday, May 15, 2017		Sheet 21	of 84
	MICRO-STAR INT'L CO.,LTD																
	MS-7A95																
	Size Custom	Document Description PCH-Strap	Rev 1.0														
Date: Monday, May 15, 2017		Sheet 21	of 84														

The diagram illustrates the PCB layout for the N11-1641491-L06 component. It shows the connection of the PE1641491-L06 component to the N11-1641491-L06 PCB. The layout includes various signal traces, power planes, and component footprints. Key components include the PE1641491-L06, N11-1641491-L06, and various passive components like resistors and capacitors. The layout is organized into sections for power, ground, and signal traces, with labels for various signals and components.

Power and Ground Connections:

- VCC3:** Connected to the PE1641491-L06 component.
- 3VSB:** Connected to the PE1641491-L06 component.
- PCH_WAKE#:** Connected to the PE1641491-L06 component.
- PE_SCL_SW_R:** Connected to the PE1641491-L06 component.
- PE_SDA_SW_R:** Connected to the PE1641491-L06 component.

Signal Connections:

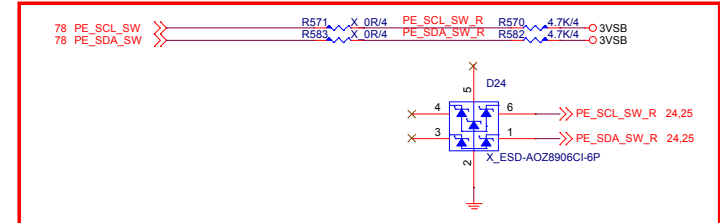
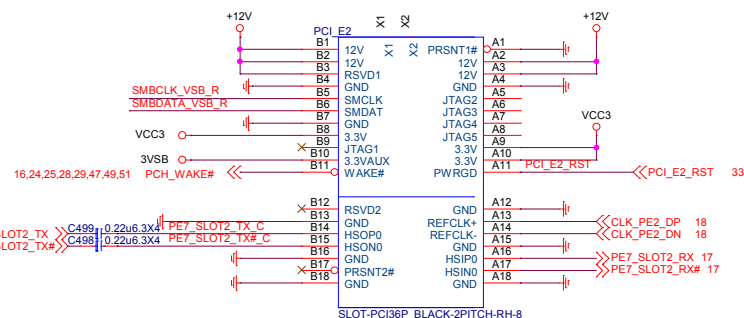
- EXP_B_TXP_15:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_15:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_14:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_14:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_13:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_13:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_12:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_12:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_11:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_11:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_10:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_10:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_9:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_9:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_8:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_8:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_7:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_7:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_6:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_6:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_5:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_5:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_4:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_4:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_3:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_3:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_2:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_2:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_1:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_1:** Connected to the PE1641491-L06 component.
- EXP_B_TXP_0:** Connected to the PE1641491-L06 component.
- EXP_B_TXN_0:** Connected to the PE1641491-L06 component.

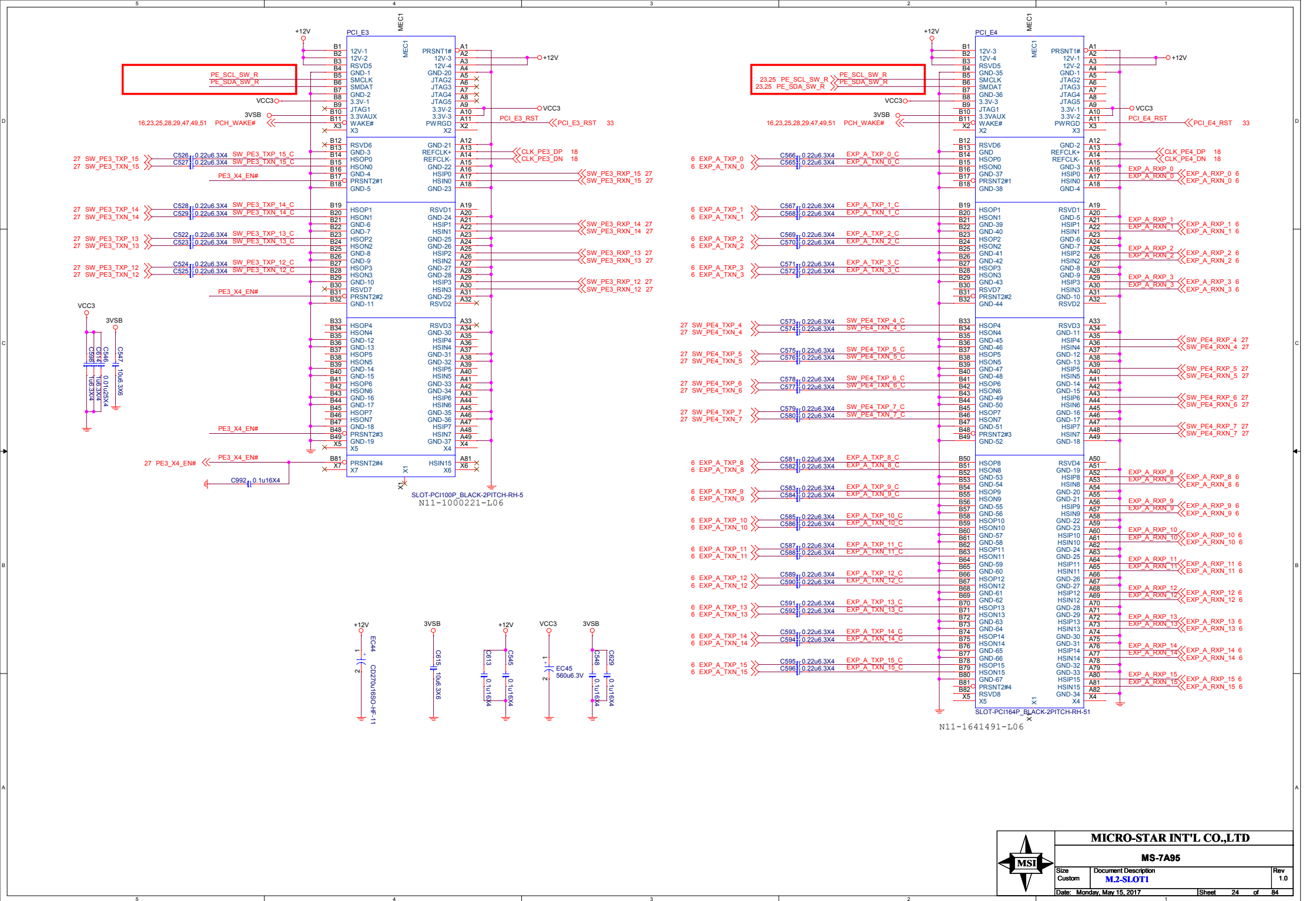
Component Footprints:

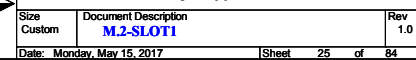
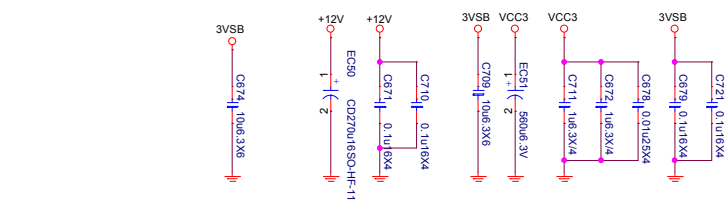
- PE1641491-L06:** The main component being connected.
- N11-1641491-L06:** The PCB component.
- Various passive components:** Resistors and capacitors used for signal conditioning and power filtering.

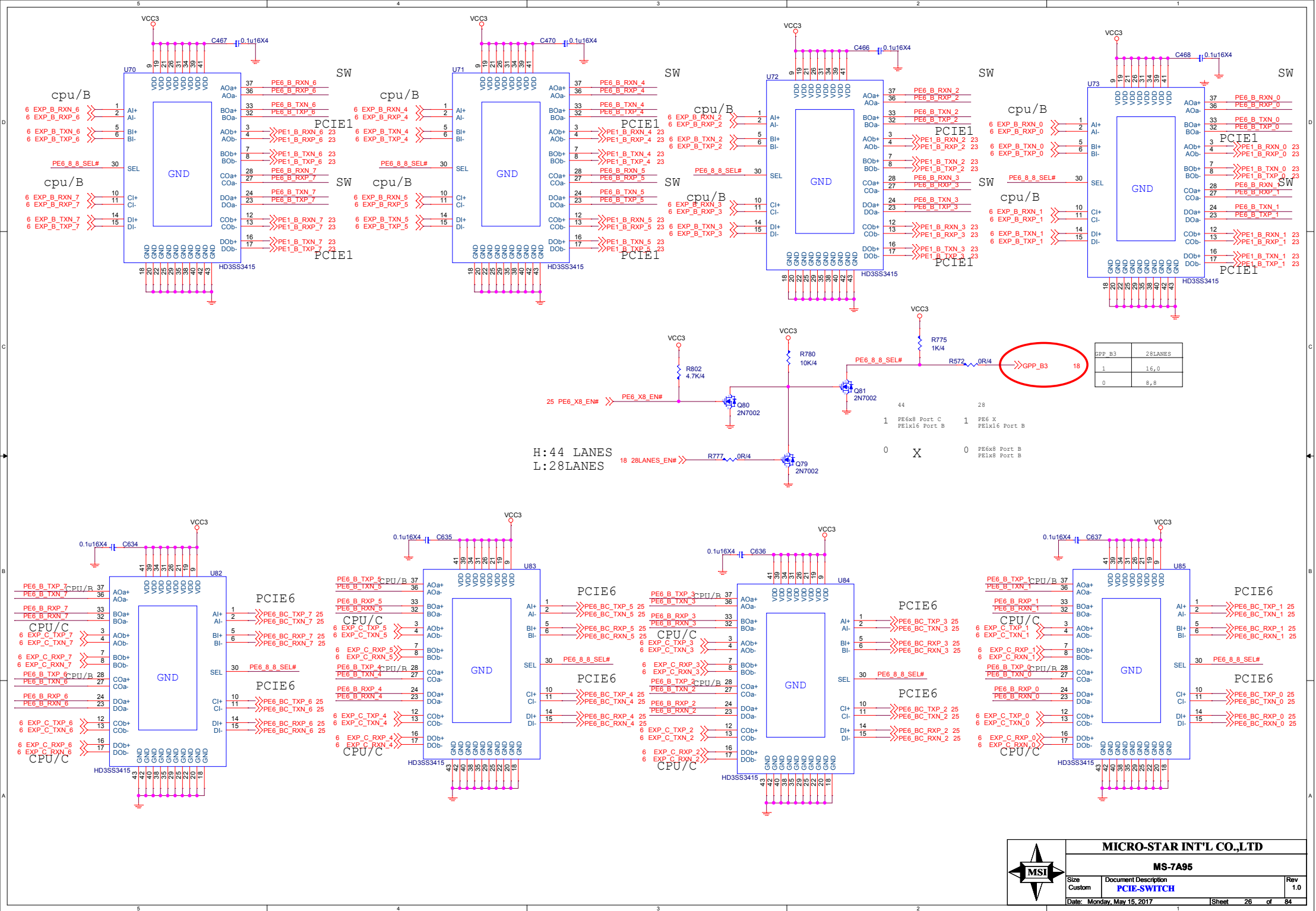
Labels and Annotations:

- 16.24.25.28.29.47.49.51:** A group of labels indicating specific signal or power connections.
- PE1641491-L06:** The component being connected.
- N11-1641491-L06:** The PCB component.
- Various signal and power labels:** Such as VCC3, 3VSB, PCH_WAKE#, PE_SCL_SW_R, PE_SDA_SW_R, EXP_B_TXP_15, EXP_B_TXN_15, etc.





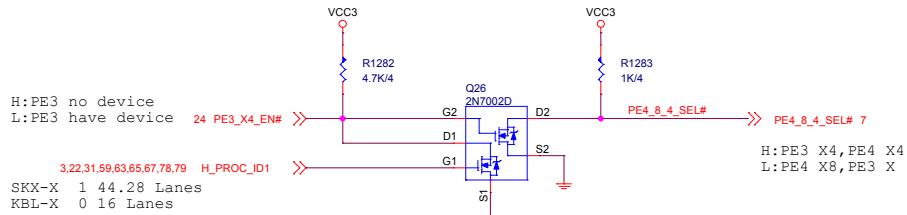
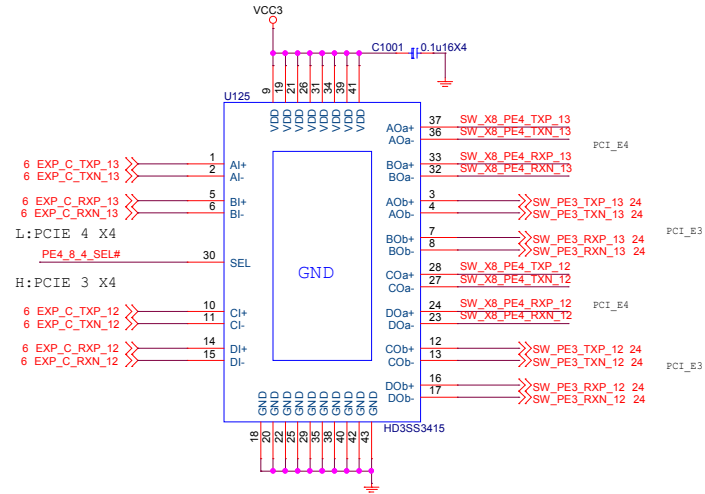
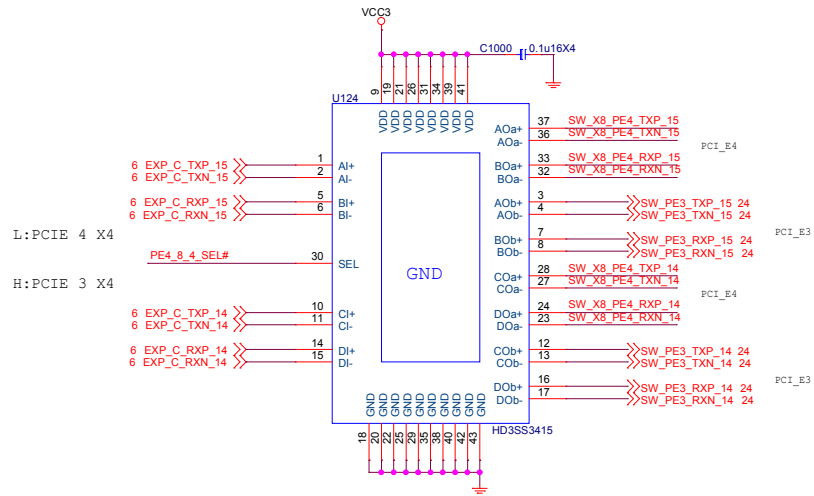
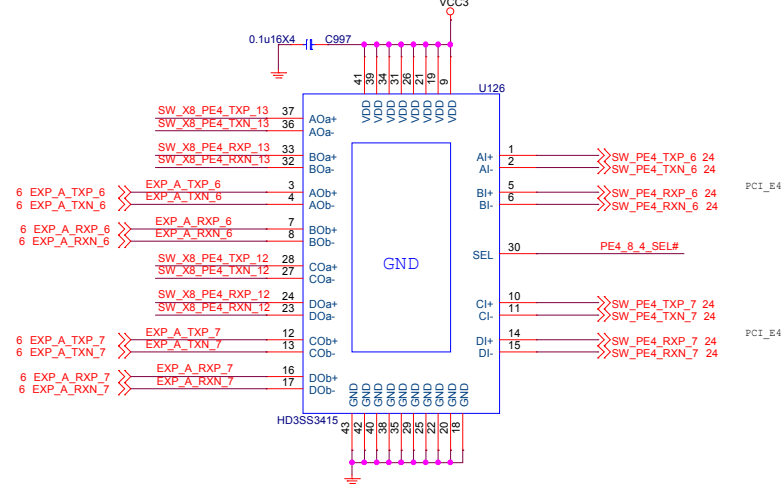
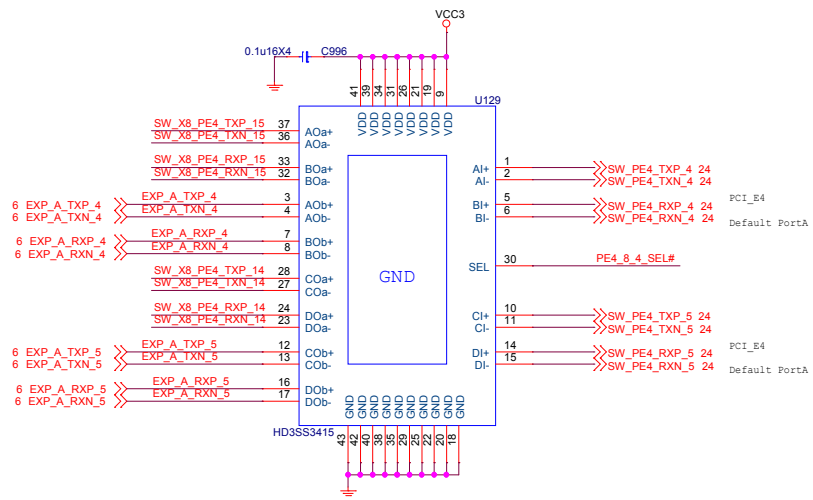


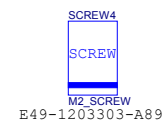


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<i>BIOS_DIS_SW2</i>	<i>BIOS_SEL_PCIESATA2</i>	<i>Mode</i>
<i>0</i>	<i>1</i>	<i>M2-SATA</i>
<i>0</i>	<i>0</i>	<i>M2-PCIE</i>
<i>GPI(1)</i>	<i>GPI(1)</i>	<i>AUTO</i>



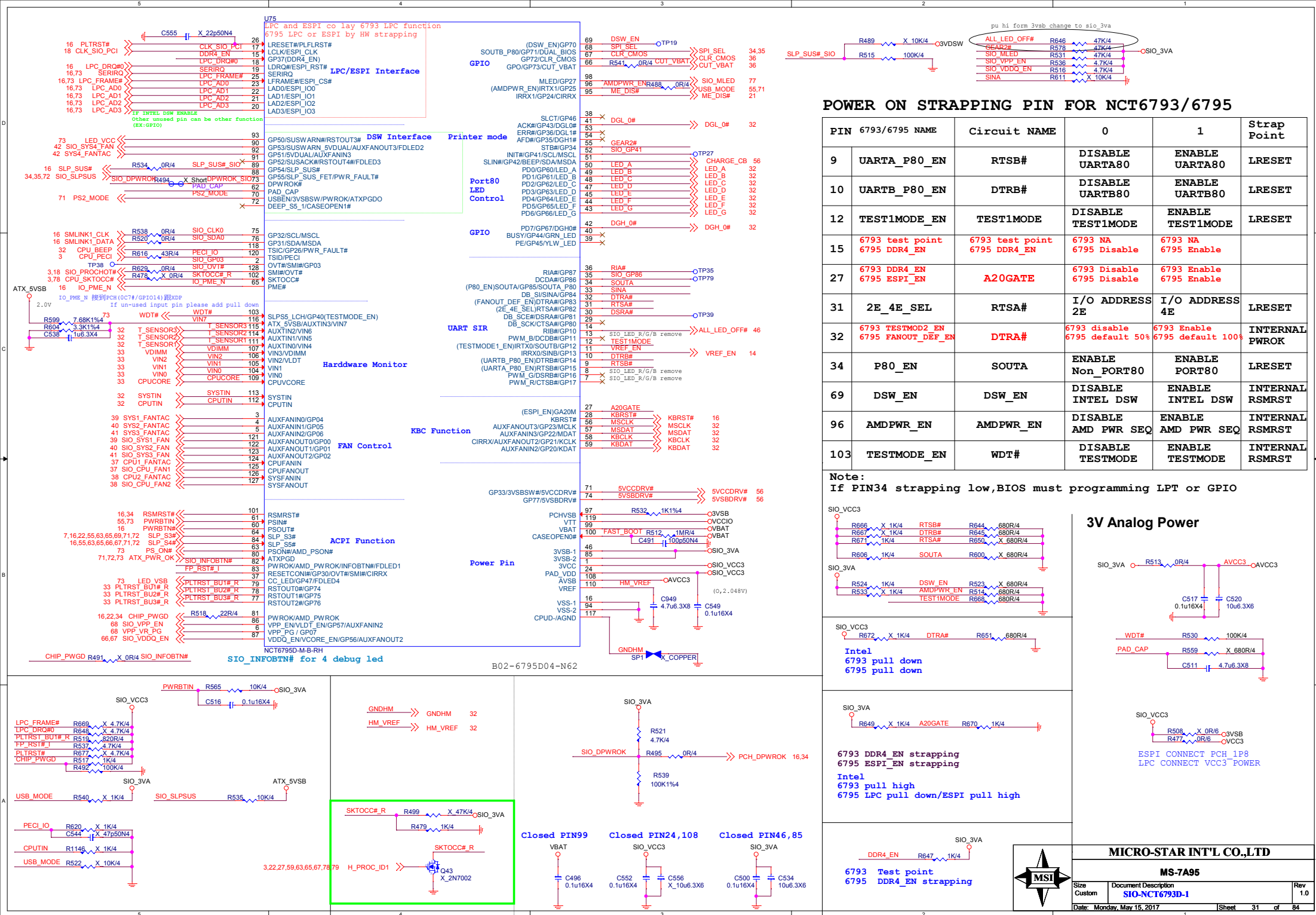
MICRO-STAR INT'L CO.,LTD

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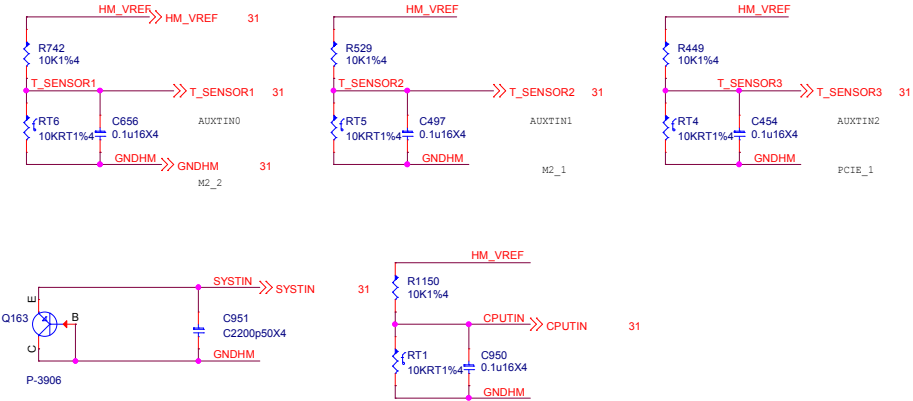
Size Custom	Document Description M.2-SLOT2
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Rev	1.0
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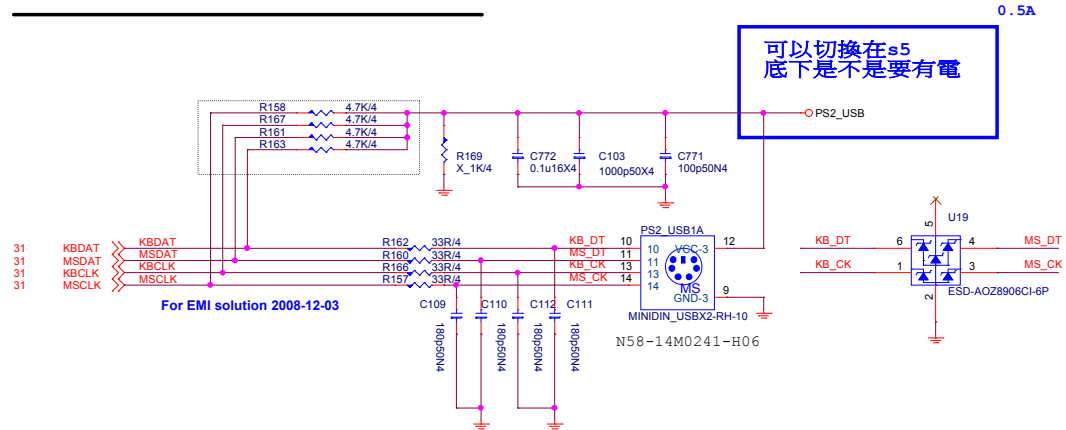
Date: Monday, May 15, 2017	Sheet 29 of 84
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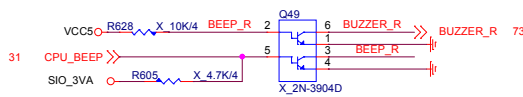
THERMAL



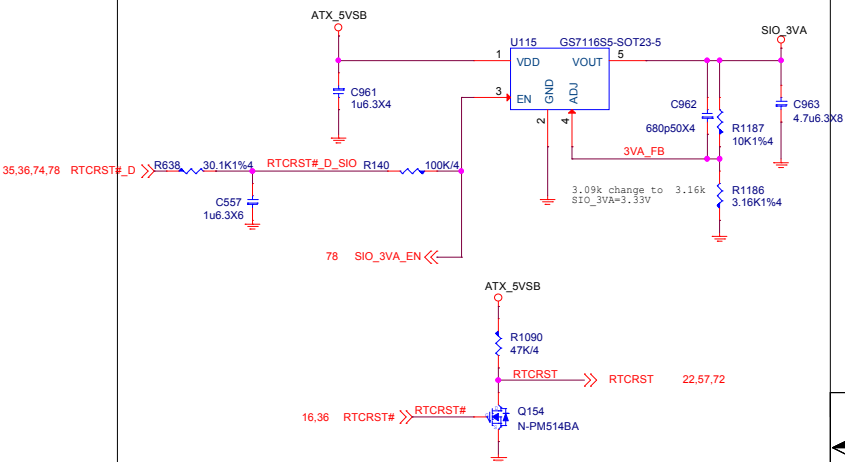
PS2 KEYBOARD & MOUSE CONNECTOR



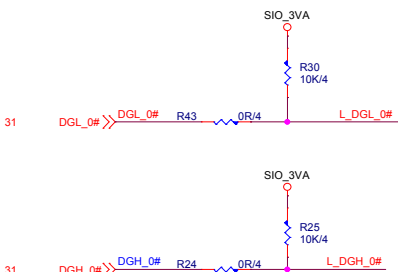
COM Port for BIOS Debug



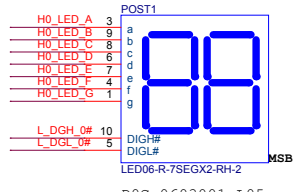
SLP_SUS Co-lay circuit



DEBUG LED



Debug LED OFF BIOS control

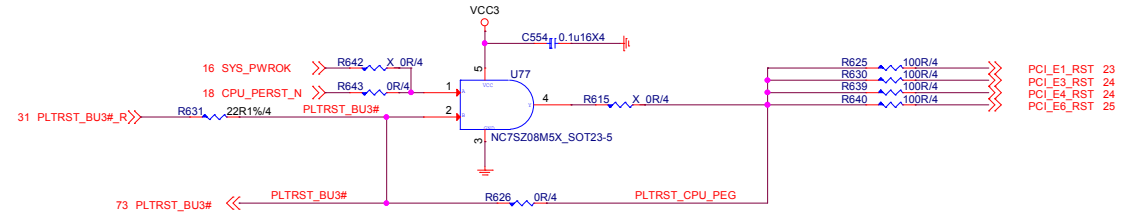
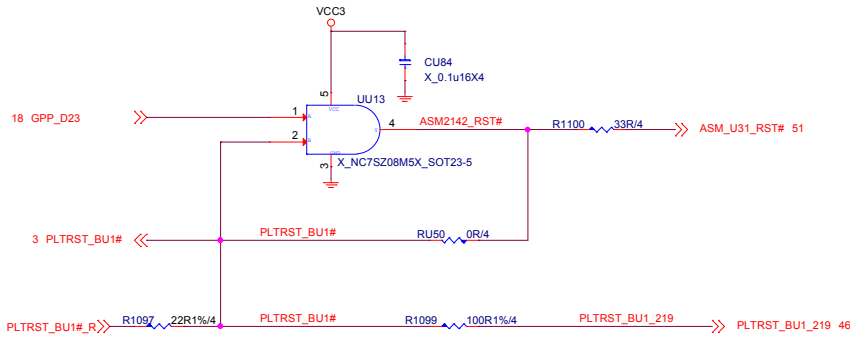
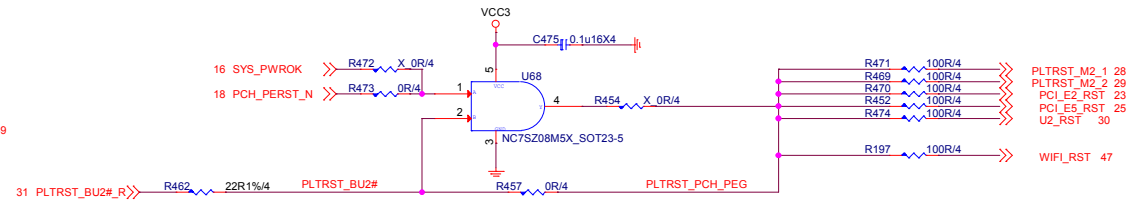
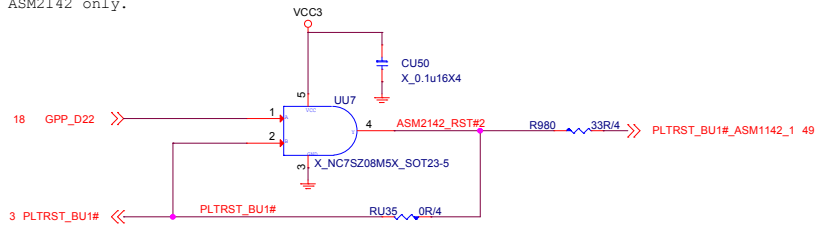


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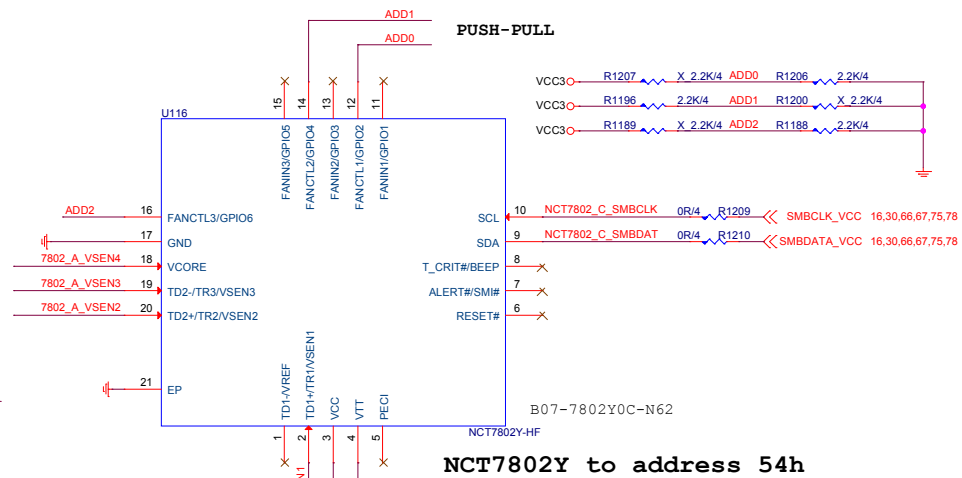
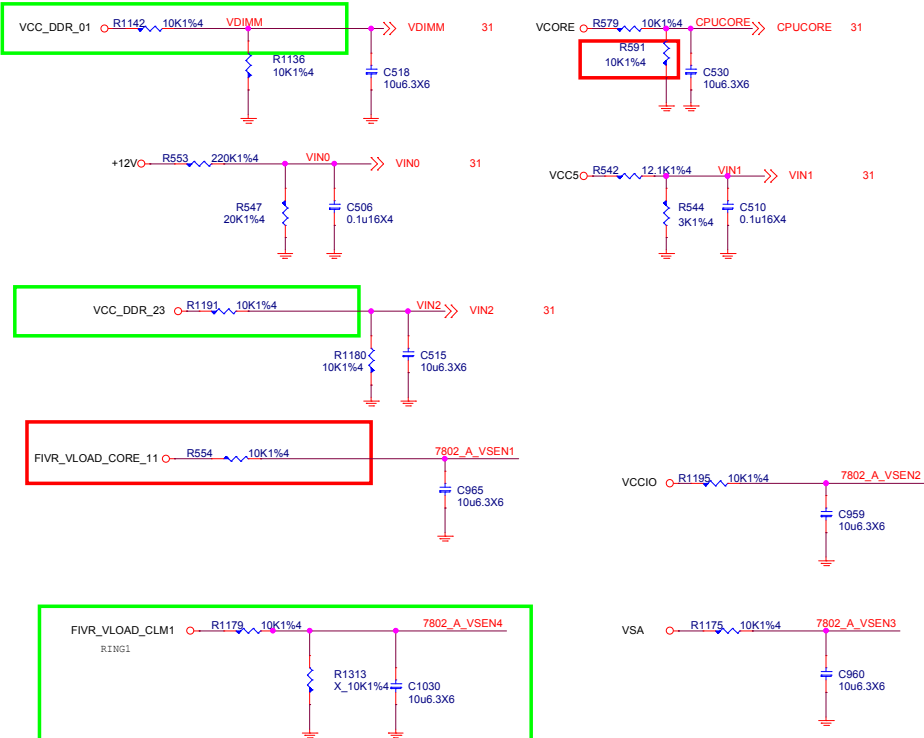
Size	Document Description	Rev
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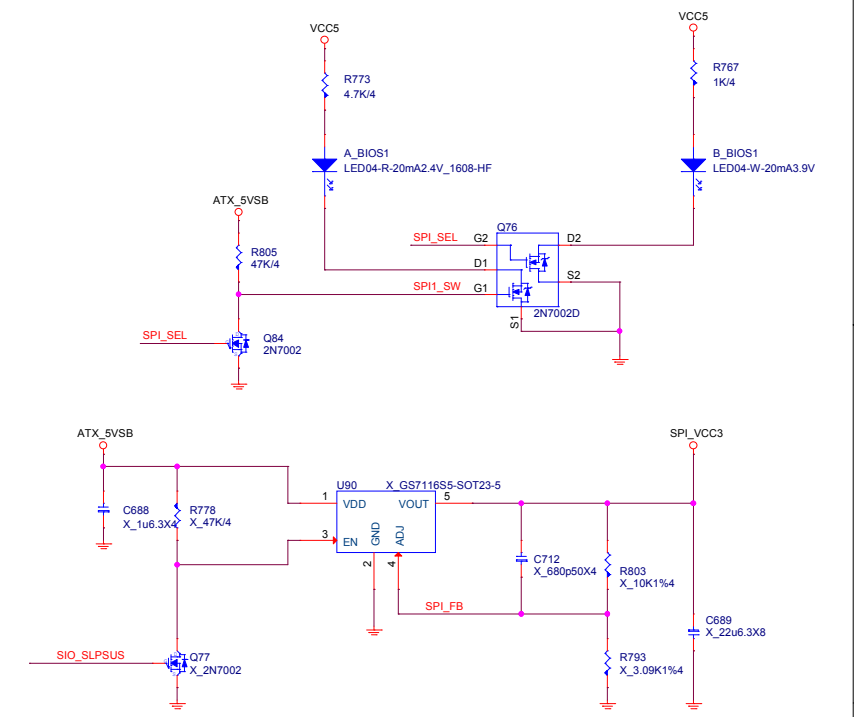
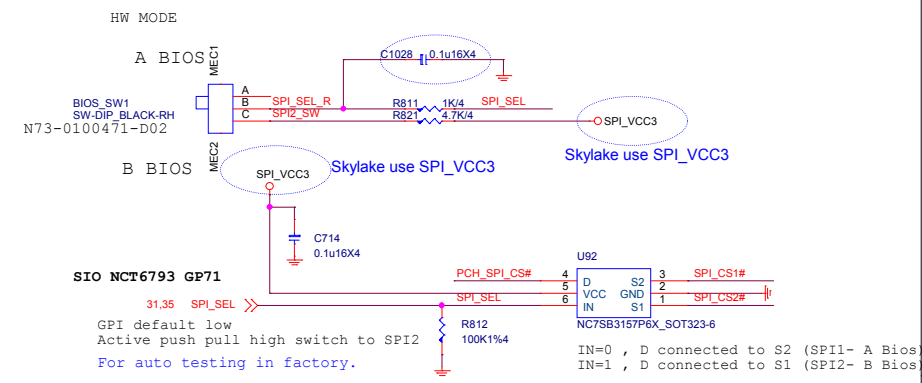
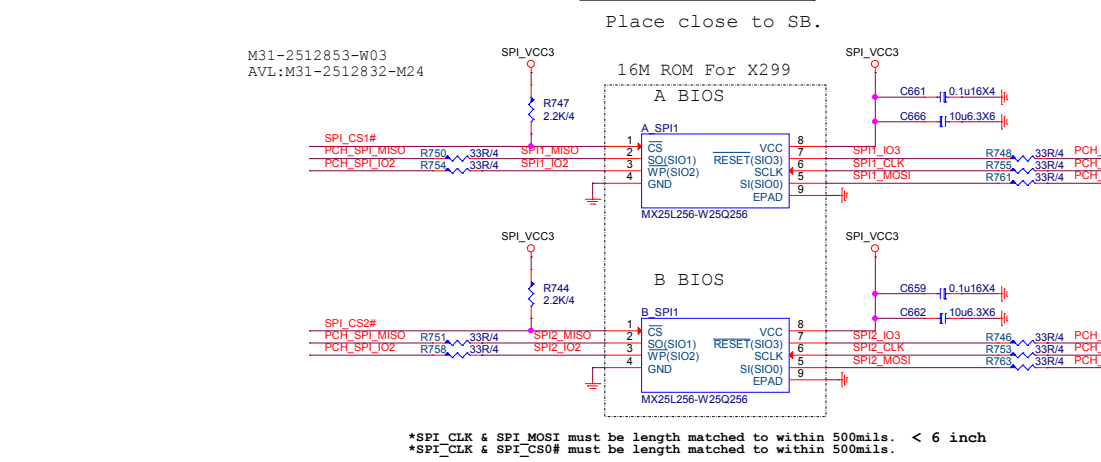
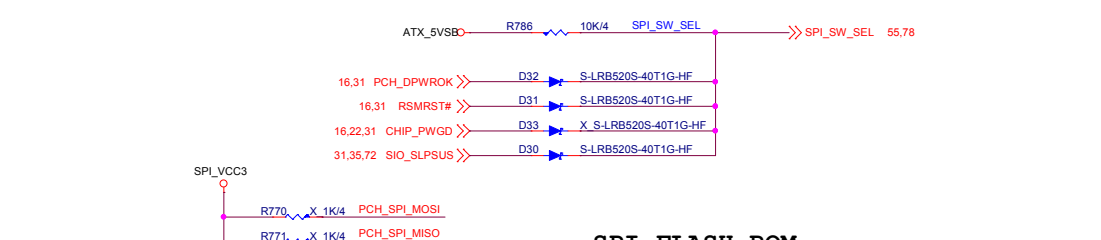
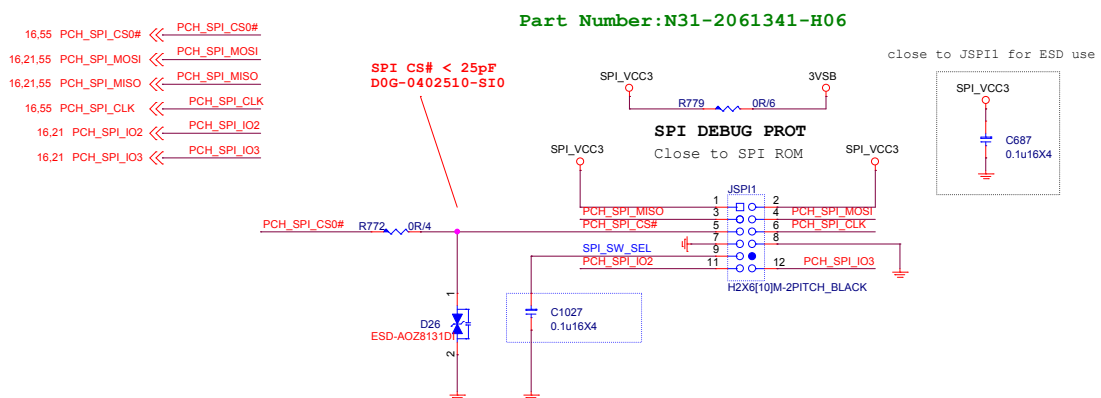
Reset control for ASM2142 only.



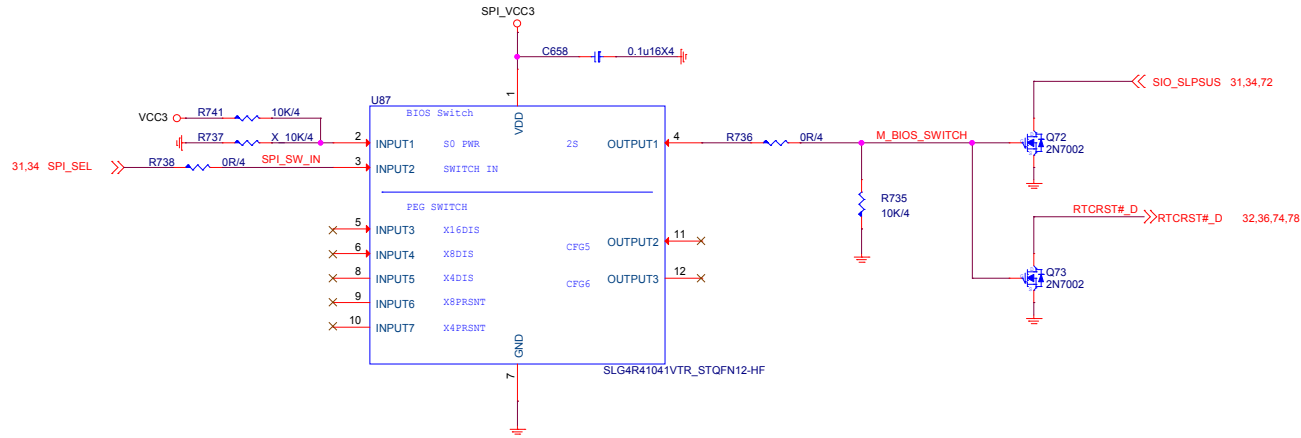
HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

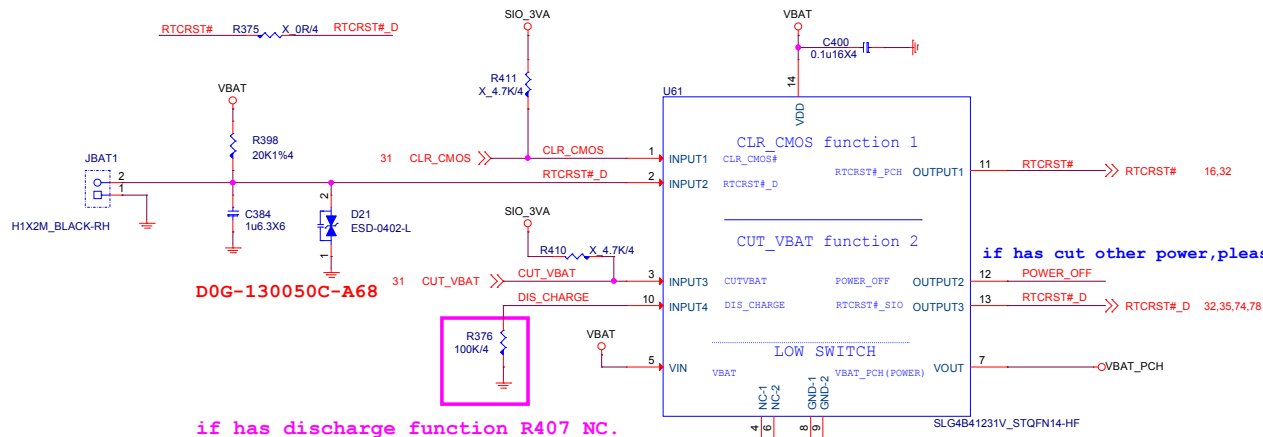
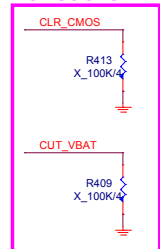




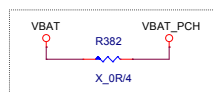
Skylake/Kabylake Path Circuit For Dual Bios



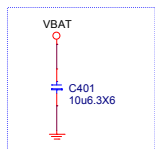
20160629



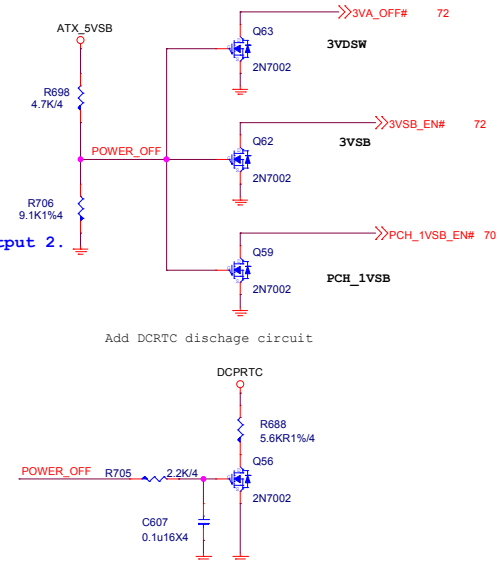
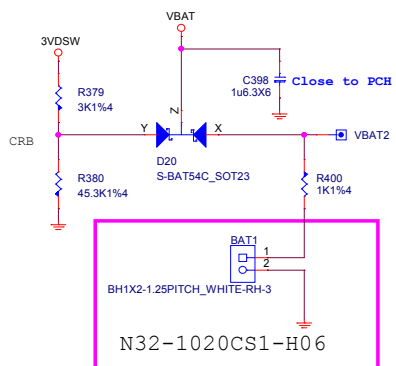
if has discharge function R407 NC.



VBAT



```
have timing issue keep
0805 size don't removed
```



TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

From SIO

31 SIO_CPU_FAN1

18 CPUFAN1_MODE

FIX MODE unstuff

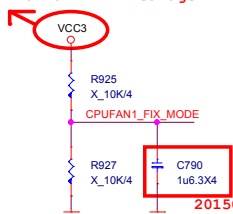
PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8*DCIN voltage.

NCT3947S-A_SOP8-HF-1

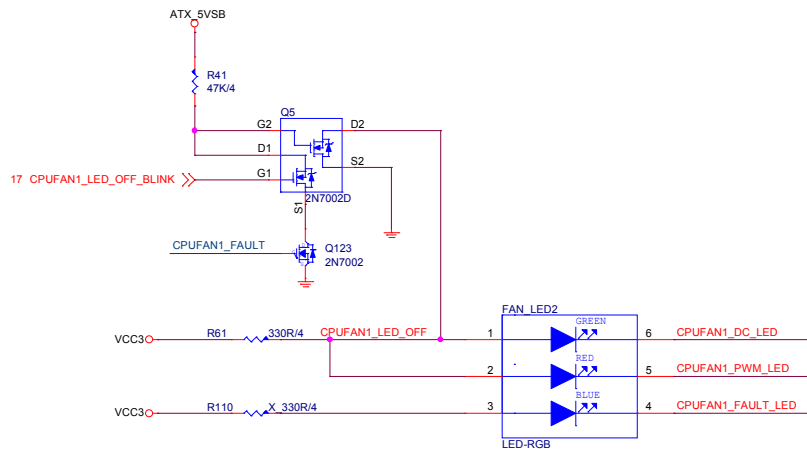
GPIO Control	
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)
Internall pull up 1.65v	

Default

Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC

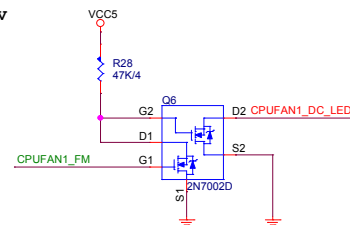


Forward Current 20mA
Pulse Forward Current 40-60mA

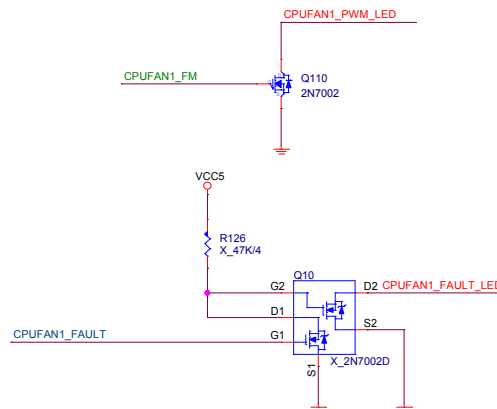
RGB
D0C-040S400-H91
DC_FAN_LED (綠)
PWM_FAN_LED (藍)
FAN_OCP_LED (紅)

CPUFAN_PWR
>40mil

C22,C23,C263 close to FAN Connector



CHECK NCT3947S Sink Current

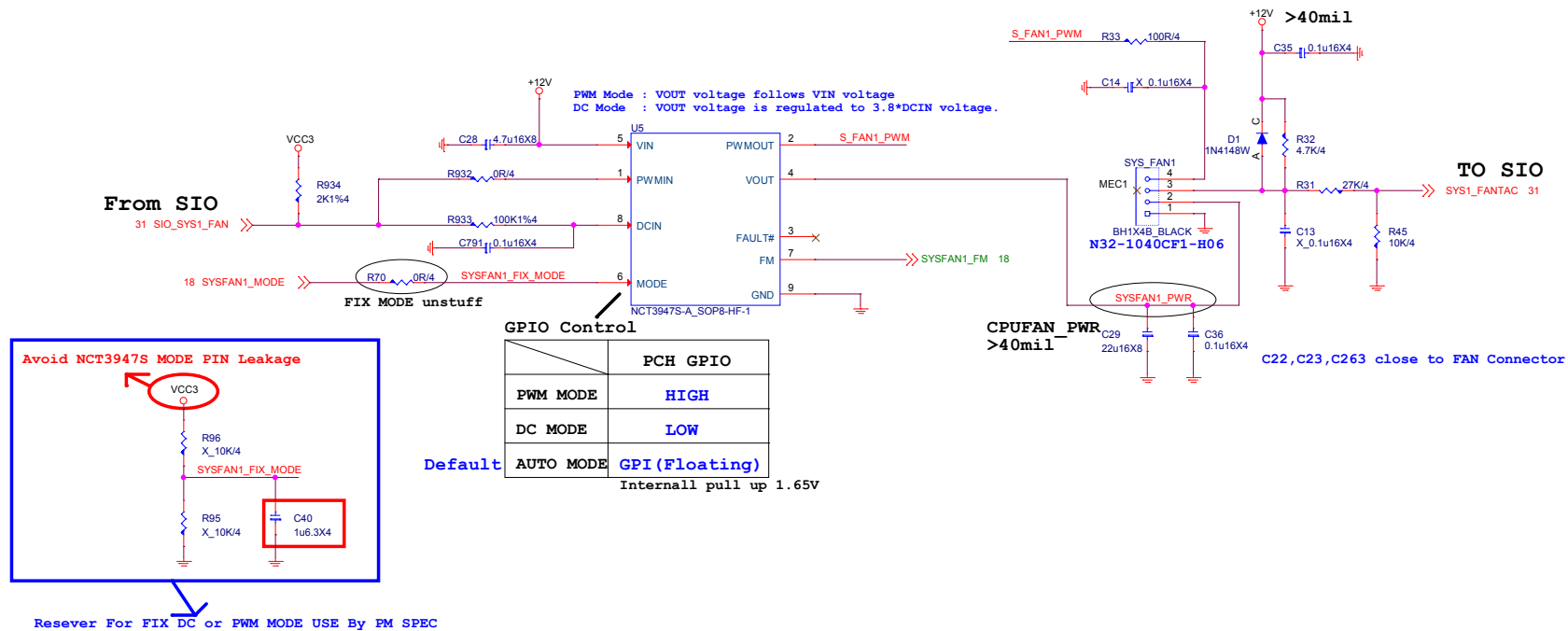


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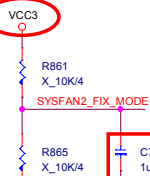
MS-7A95

Size Custom	Document Description CPU FAN1	Rev 1.0
Date: Monday, May 15, 2017	Sheet 37 of 84	

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



31 SIO_SYS2_FAN >>

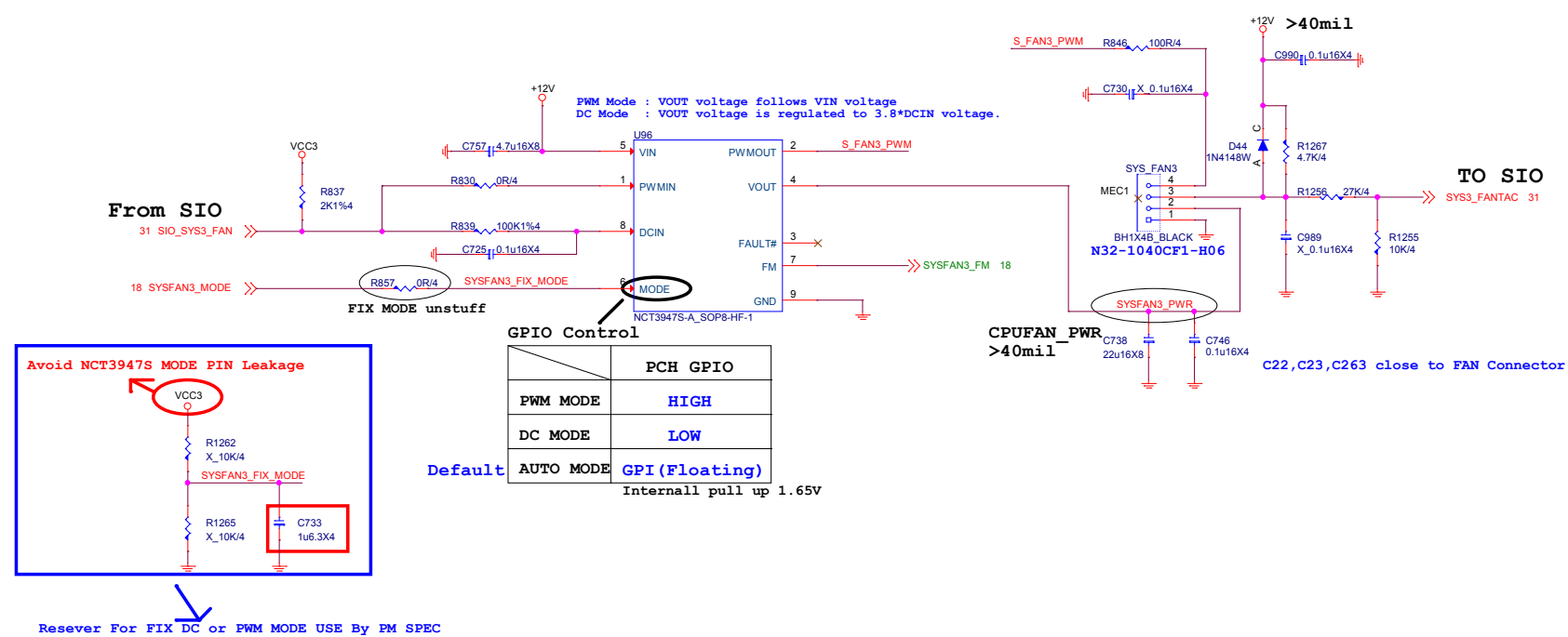


Resever For FIX DC or PWM MODE USE By PM SPEC

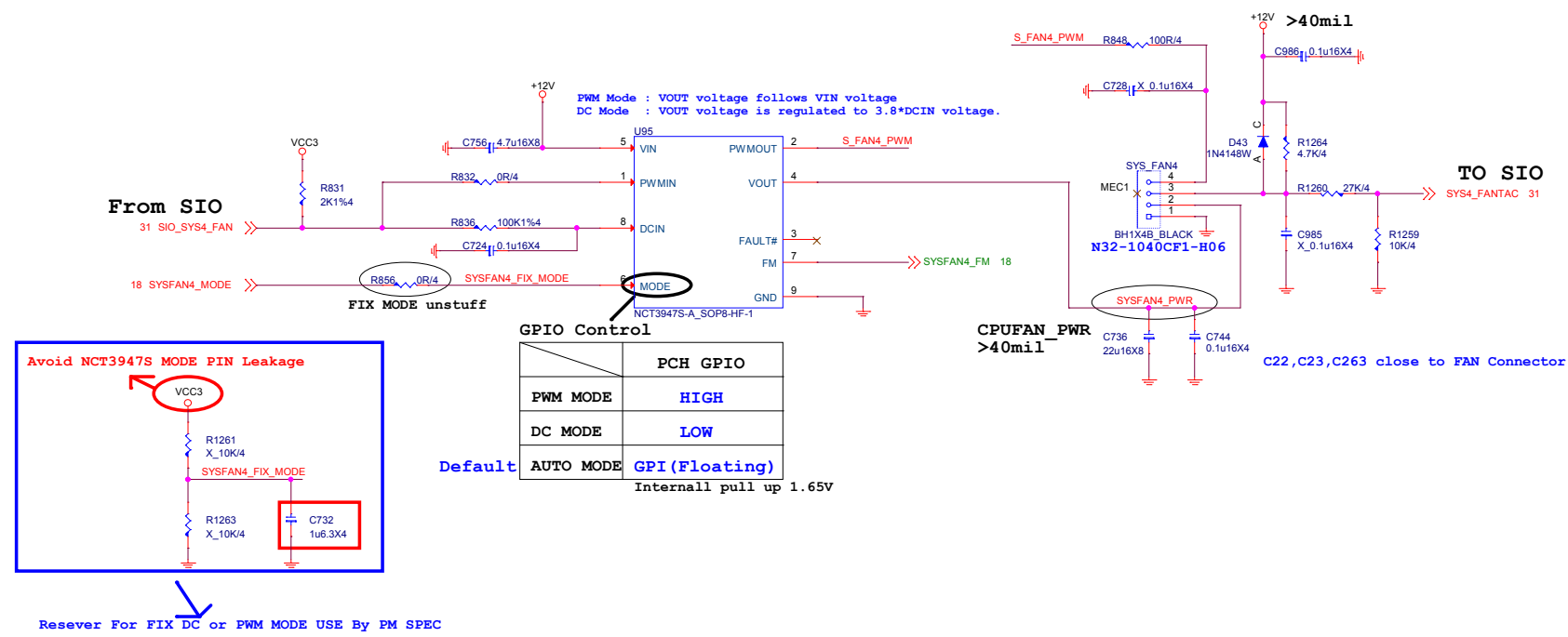
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPIO(Floating)

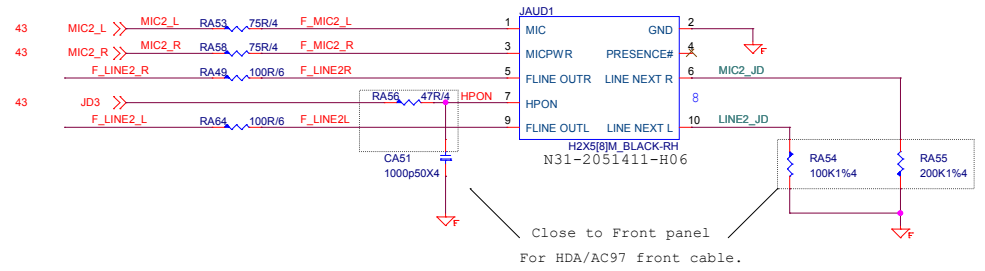
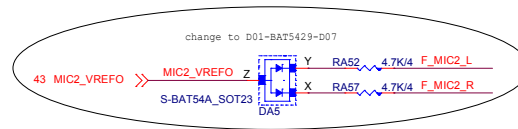
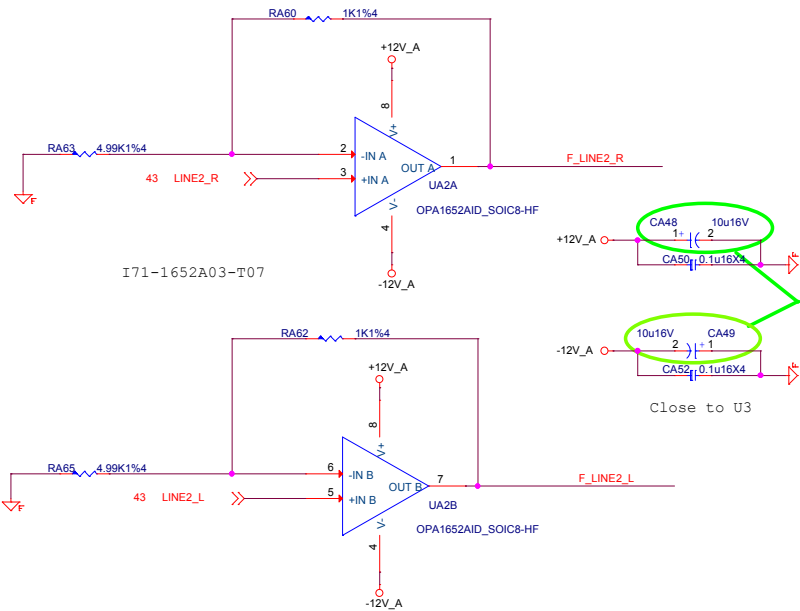
Internall pull up 1.65V

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

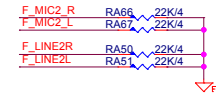
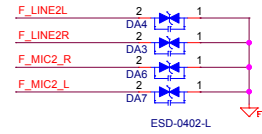


TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

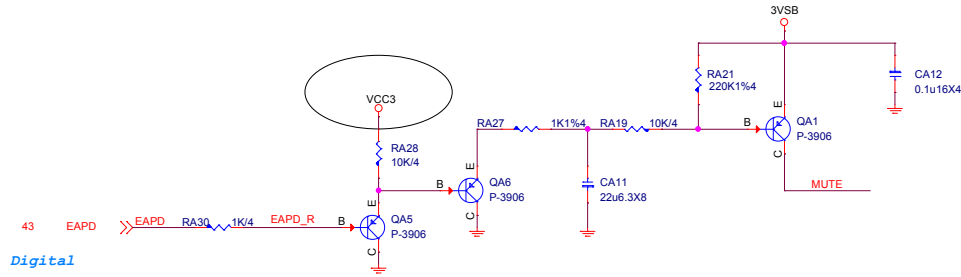




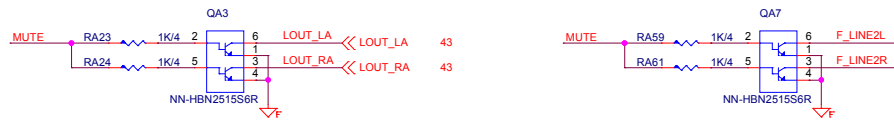
Close to Jack
ESD protect
 D0G-2950500-SI0
 D0G-3010510-I05



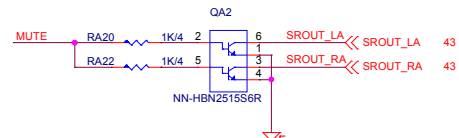
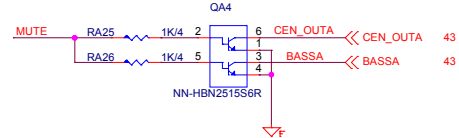
Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

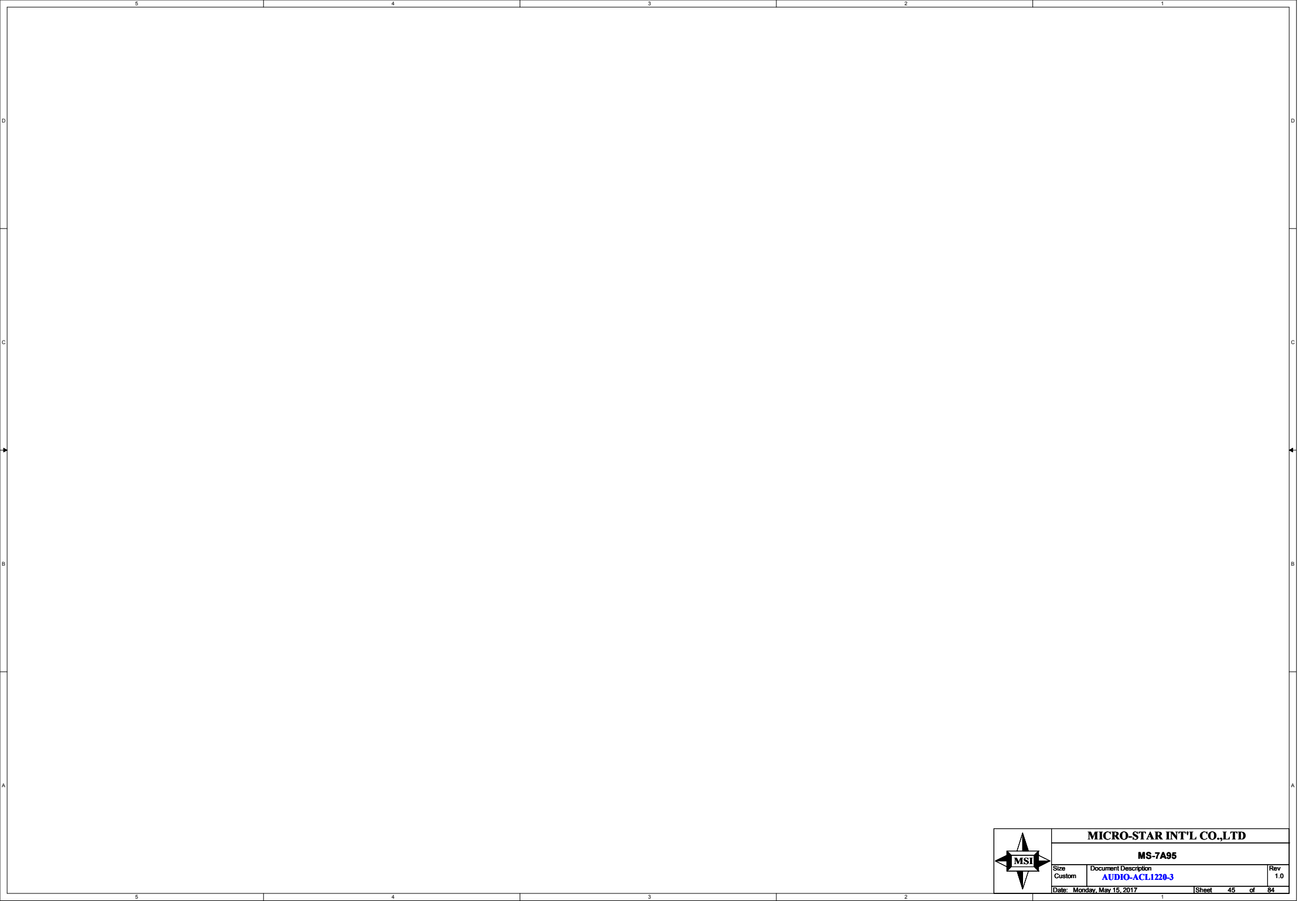


Analog



(add de-pop circuit by PM spec or customer request,
 NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



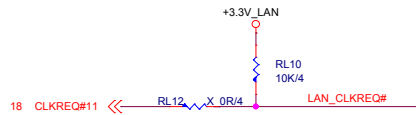
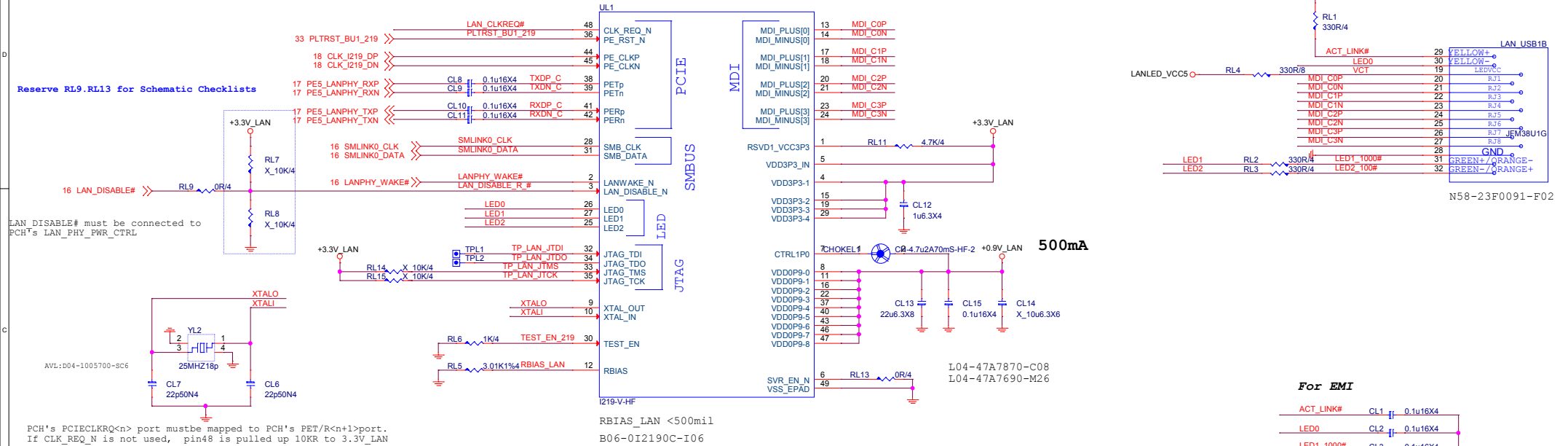


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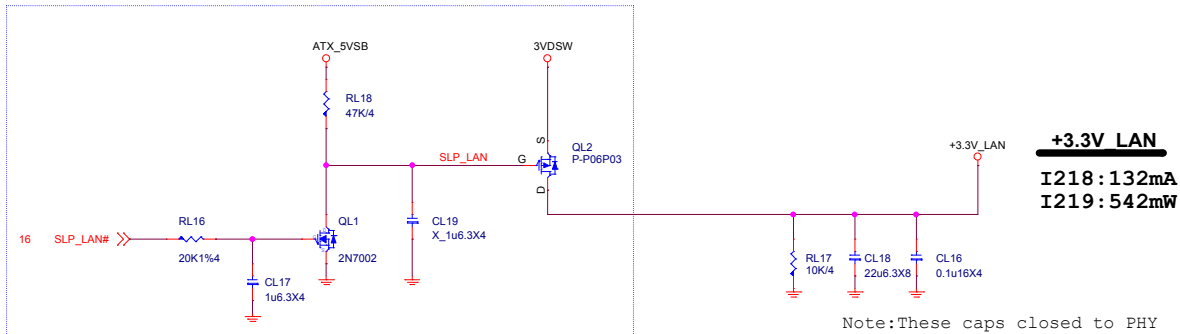
Size Custom	Document Description AUDIO-ACL1220-3	Rev 1.0
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Intel I219V / I218V PHY

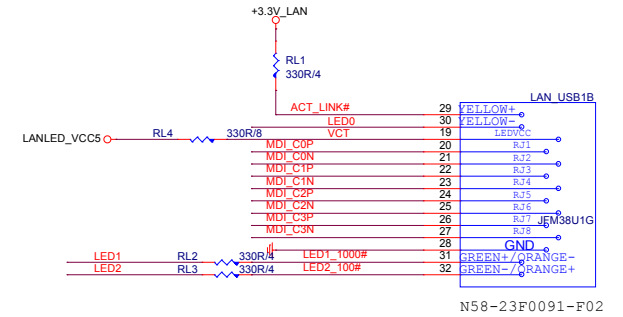


The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

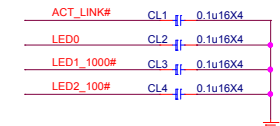
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



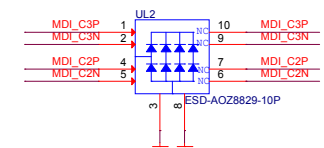
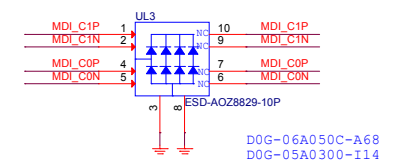
Note: These caps closed to PHY



For EMI



UL2&UL3 close to connector



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Size Custom	Document Description Intel Lan- i219	Rev 1.0
Date: Monday, May 15, 2017		Sheet 46 of 84

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole <2

[illegible][illegible]

The diagram shows the SPI connection between the STM32F407 and the M31-25L1022-M24. The STM32F407's VCC3 pin is connected to the M31-25L1022-M24's VCC pin (pin 8). The STM32F407's RU11 pin is connected to the M31-25L1022-M24's CS pin (pin 1) through a 10K/4 resistor. The STM32F407's RU12 pin is connected to the M31-25L1022-M24's SI pin (pin 5) through a 4.7K/4 resistor. The STM32F407's RU9 pin is connected to the M31-25L1022-M24's SO pin (pin 2) through a 4.7K/4 resistor. The STM32F407's RU7 pin is connected to the M31-25L1022-M24's SCK pin (pin 6) through a 4.7K/4 resistor. A 0.1uF/6X4 capacitor is connected between VCC3 and GND.

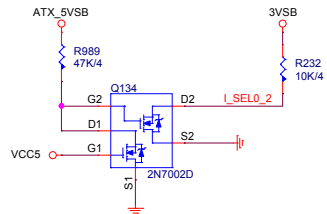
M31-25L1022-M24 (1M)
AVL:M31-25X2023-W03 (2M)



MS-7A95

Size Custom	Document Description 49.ASM2142AE REAL-USB31-1	Rev 1.0
Date: Tuesday, May 16, 2017		Sheet 49 of 84

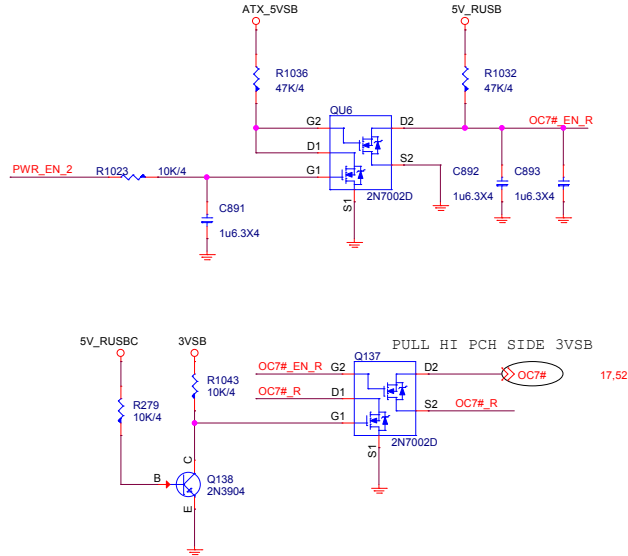
Current Mode



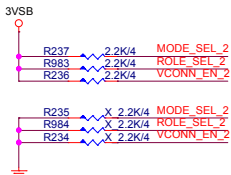
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

VBUS OC#



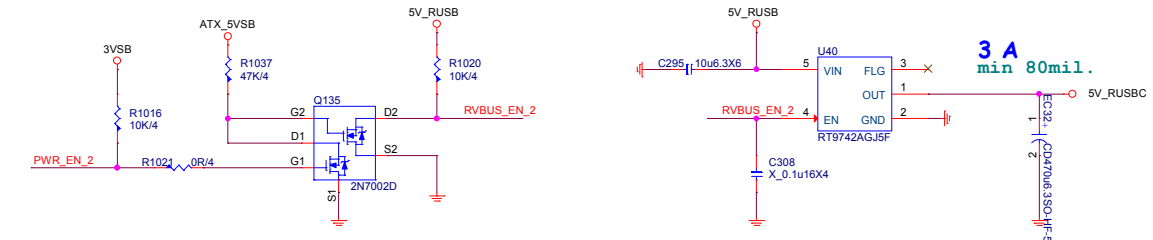
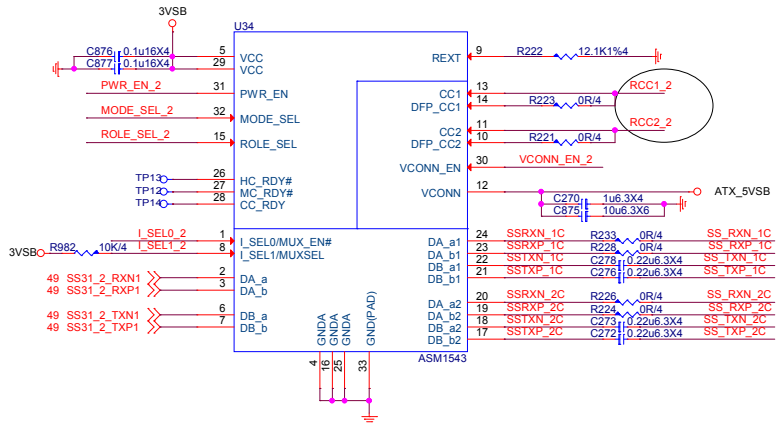
USB Type-C MUX with Configuration Channel (CC)



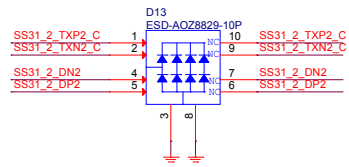
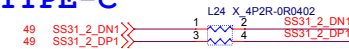
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

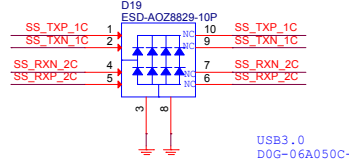
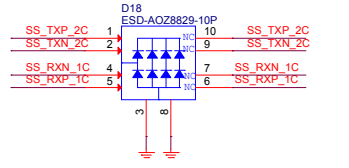
VCONN_EN	
1	enable
0	disable



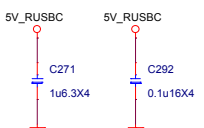
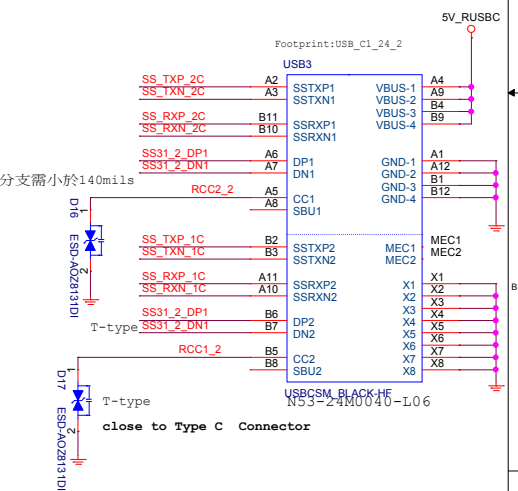
TYPE-C



ESD Protection
NEAR CONNECTOR



USB3.0
DQG-06A050C-A68 Main
DQG-05A0300-I14 AVL
DQG-45B031C-005 AVL



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Size	Document Description	Rev	
Custom	USB TYPEC-A-2	1.0	
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Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2



The image shows a detailed PCB layout for a USB3.1 Gen1 to SATA6G adapter. The central component is the ASM2142 USB3.1 Gen1 controller. The layout includes various power and signal traces, component footprints, and labels for components like CU24, YU2, and CU36. The USB3.1 Gen1 connector is labeled 'USB3.1 Gen1' and the SATA6G controller is labeled 'SATA6G'.

USB3.1 Gen1 Connector:

- 13: VREGIN
- 14: LXI
- 16: VCCHSUS_IN
- 17: VDDSSUS_O
- 20: VCCLU-1
- 24: VDDSSUS-1
- 21: VDDSSUS-2
- 65: GND
- 15: PGND

ASM2142-1A1-RH Pinout:

- 4: VCC3
- 55: USB3_3VCC_2P5
- 38: USB3_1P2
- 1: VDD-1
- 12: VDD-2
- 33: VDD-3
- 52: VDDP-1
- 58: VDDP-2
- 35: VDDU-1
- 41: VDDU-2
- 47: VDDU-3

SATA6G Connector:

- 1: SATA6G_1
- 2: SATA6G_2
- 3: SATA6G_3
- 4: SATA6G_4
- 5: SATA6G_5
- 6: SATA6G_6
- 7: SATA6G_7
- 8: SATA6G_8
- 9: SATA6G_9
- 10: SATA6G_10
- 11: SATA6G_11
- 12: SATA6G_12
- 13: SATA6G_13
- 14: SATA6G_14
- 15: SATA6G_15
- 16: SATA6G_16
- 17: SATA6G_17
- 18: SATA6G_18
- 19: SATA6G_19
- 20: SATA6G_20
- 21: SATA6G_21
- 22: SATA6G_22
- 23: SATA6G_23
- 24: SATA6G_24
- 25: SATA6G_25
- 26: SATA6G_26
- 27: SATA6G_27
- 28: SATA6G_28
- 29: SATA6G_29
- 30: SATA6G_30
- 31: SATA6G_31
- 32: SATA6G_32
- 33: SATA6G_33
- 34: SATA6G_34
- 35: SATA6G_35
- 36: SATA6G_36
- 37: SATA6G_37
- 38: SATA6G_38
- 39: SATA6G_39
- 40: SATA6G_40
- 41: SATA6G_41
- 42: SATA6G_42
- 43: SATA6G_43
- 44: SATA6G_44
- 45: SATA6G_45
- 46: SATA6G_46
- 47: SATA6G_47
- 48: SATA6G_48
- 49: SATA6G_49
- 50: SATA6G_50
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- 53: SATA6G_53
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- 58: SATA6G_58
- 59: SATA6G_59
- 60: SATA6G_60
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- 62: SATA6G_62
- 63: SATA6G_63
- 64: SATA6G_64
- 65: SATA6G_65
- 66: SATA6G_66
- 67: SATA6G_67
- 68: SATA6G_68
- 69: SATA6G_69
- 70: SATA6G_70
- 71: SATA6G_71
- 72: SATA6G_72
- 73: SATA6G_73
- 74: SATA6G_74
- 75: SATA6G_75
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- 77: SATA6G_77
- 78: SATA6G_78
- 79: SATA6G_79
- 80: SATA6G_80
- 81: SATA6G_81
- 82: SATA6G_82
- 83: SATA6G_83
- 84: SATA6G_84
- 85: SATA6G_85
- 86: SATA6G_86
- 87: SATA6G_87
- 88: SATA6G_88
- 89: SATA6G_89
- 90: SATA6G_90
- 91: SATA6G_91
- 92: SATA6G_92
- 93: SATA6G_93
- 94: SATA6G_94
- 95: SATA6G_95
- 96: SATA6G_96
- 97: SATA6G_97
- 98: SATA6G_98
- 99: SATA6G_99
- 100: SATA6G_100

VCC3

RU23 10K/4

RU42 10K/4

USB_SPICSB

USB_SPISO

RU46 X 4.7K/4

USB_SPISCK

CU32 0.1u16X4

VCC3

7

8

4

1

2

3

4

5

6

U12

HOLD

WP

CS

VCC

GND

SI

SO

SCK

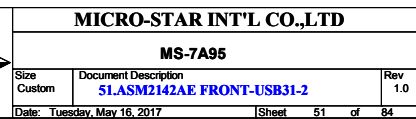
M31-25L1022-M24

RU48 X 4.7K/4

USB_SPISO

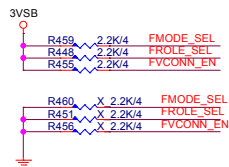
M31-25L1022-M24

AVL: M31-25X2023-W03



USB 3.1-Type-C

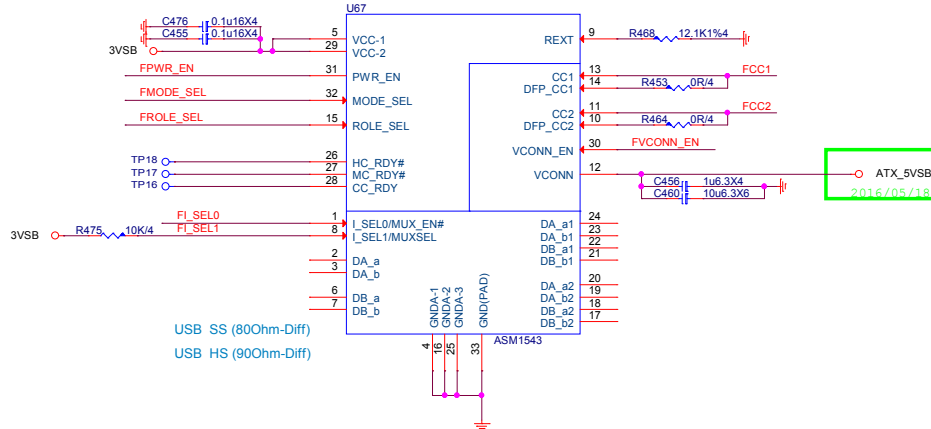
USB Type-C MUX with Configuration Channel (CC)



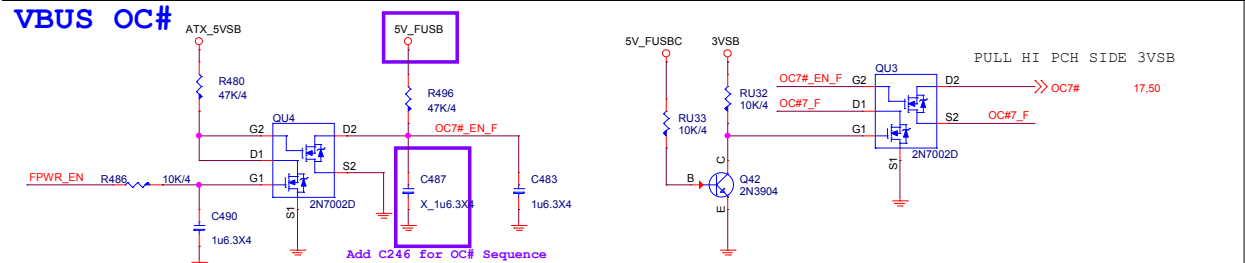
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

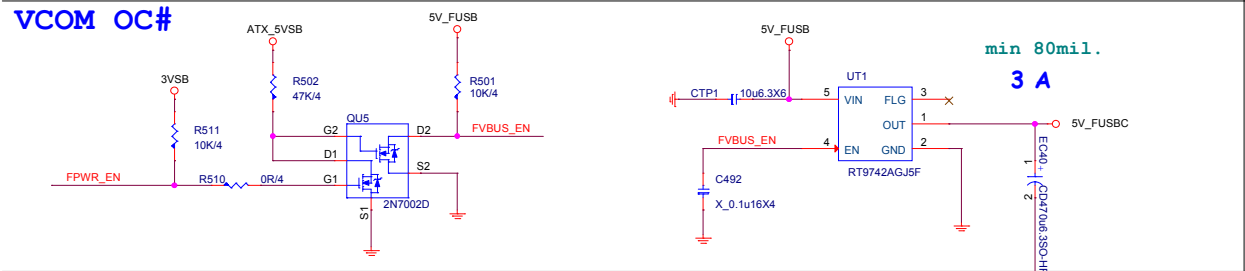
VCONN_EN	
1	enable
0	disable



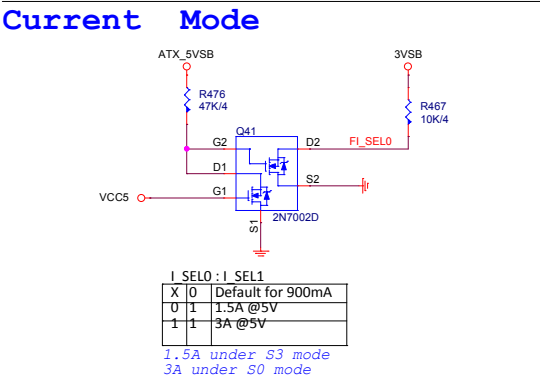
VBUS OC#



VCOM OC#

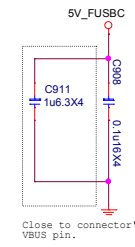
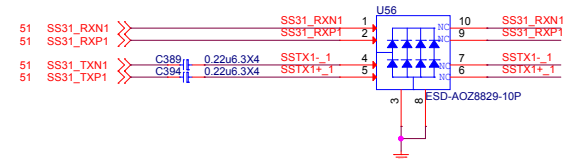
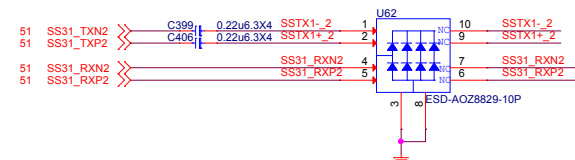
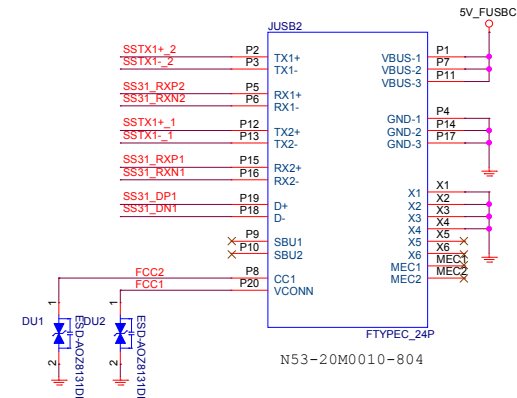
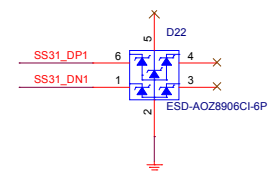


Current Mode



I_SEL0 : I_SEL1	
X 0	Default for 900mA
0 1	1.5A @5V
1 1	3A @5V

1.5A under S3 mode
3A under S0 mode



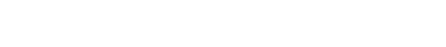
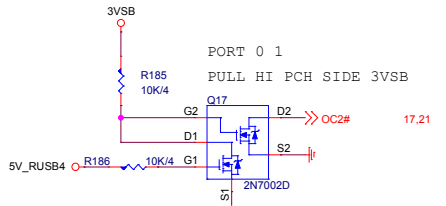
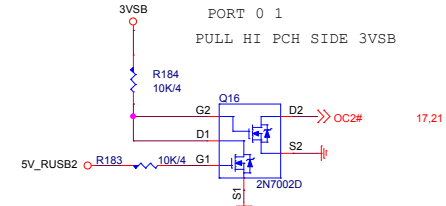
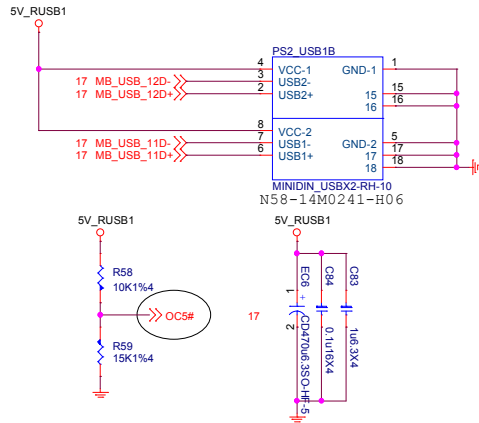
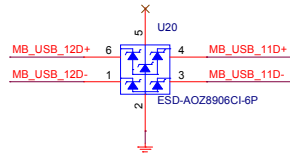
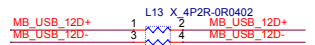
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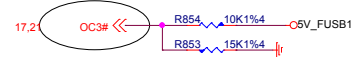
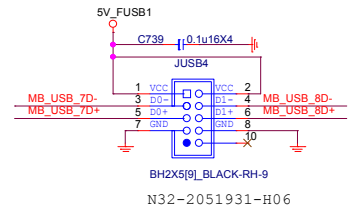
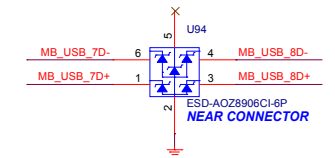
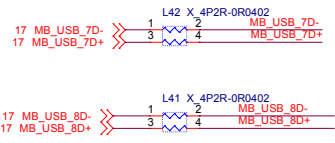
Size Custom Document Description **USB FRONT TYPE-C** Rev 1.0

Date: Monday, May 15, 2017 Sheet 52 of 84

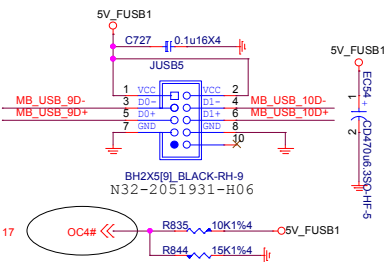
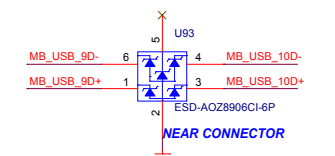
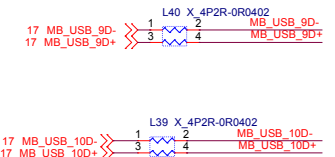
PS2_USB1



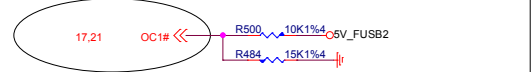
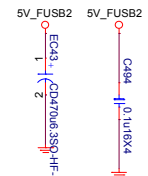
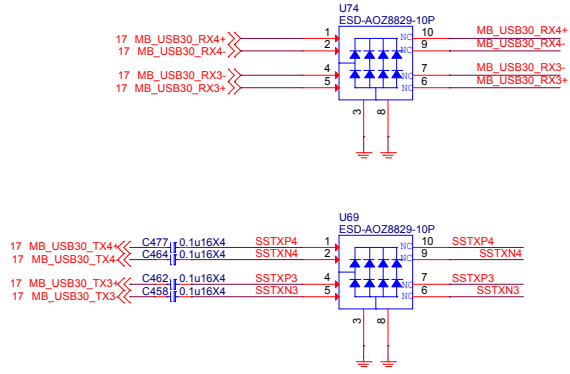
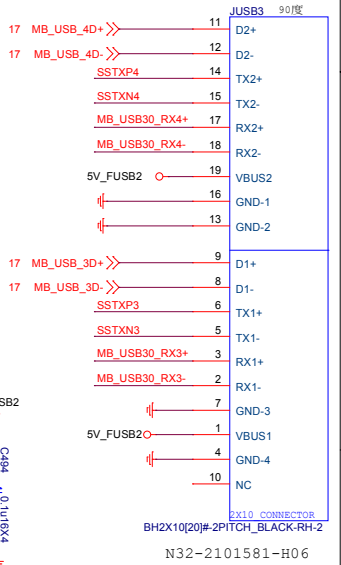
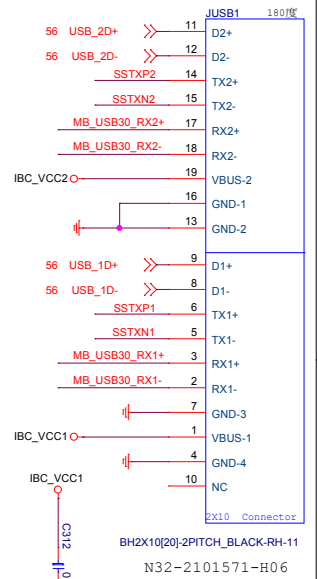
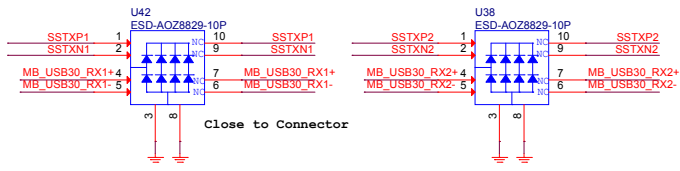
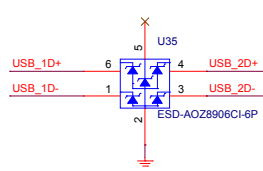
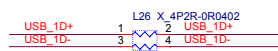
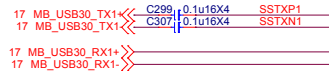
FRONT USB PORT 7,8



FRONT USB PORT 9,10



0D先Remove Redriver



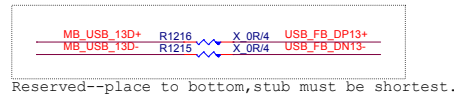
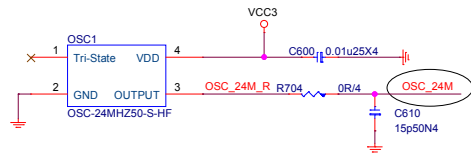
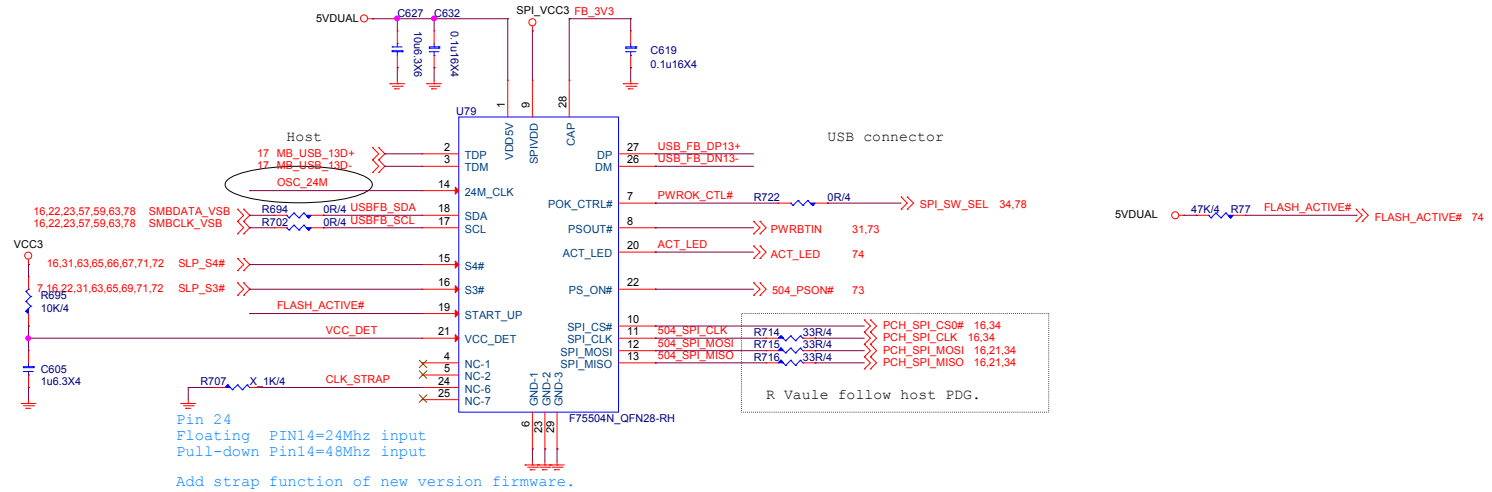
MICRO-STAR INT'L CO.,LTD

MS-7A95

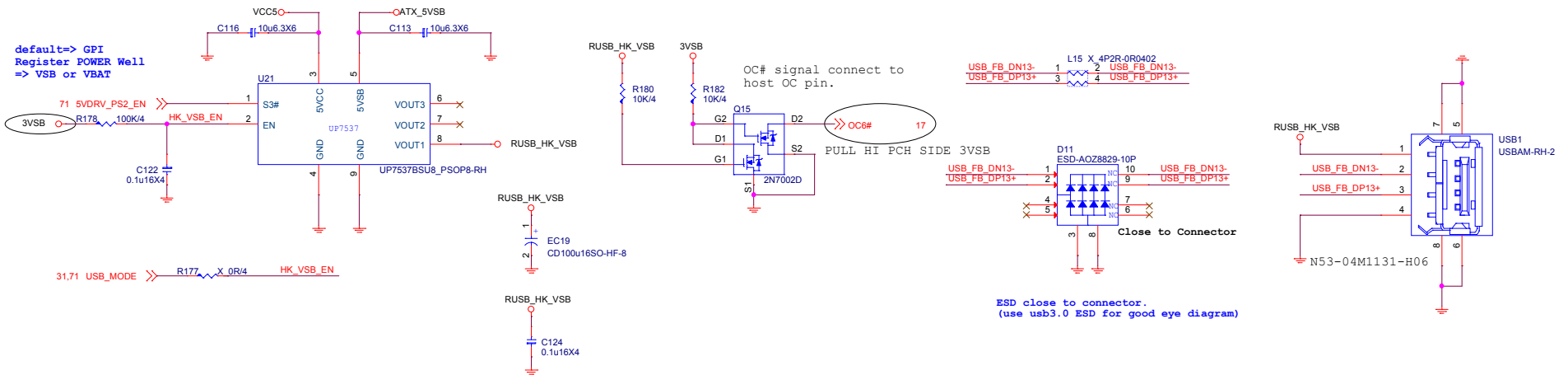
Size	Document Description	Rev
Custom	Rear/Front USB2.0	1.0
Date: Monday, May 15, 2017	Sheet 54 of 84	

Host USB connector

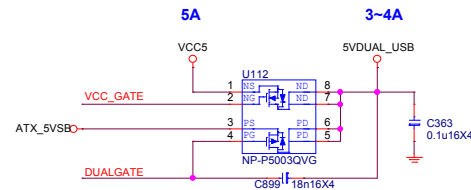
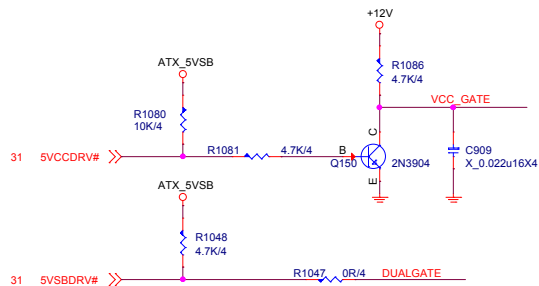
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



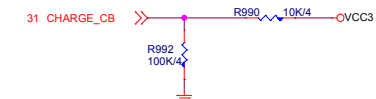
USB Connector power come from UP7537
provide(USB Hotkey Connector same)



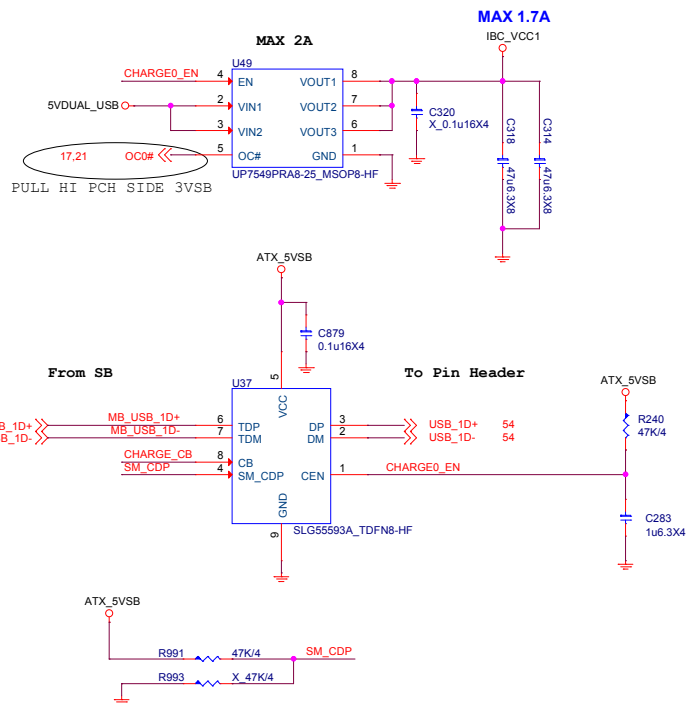
5VDUAL_USB



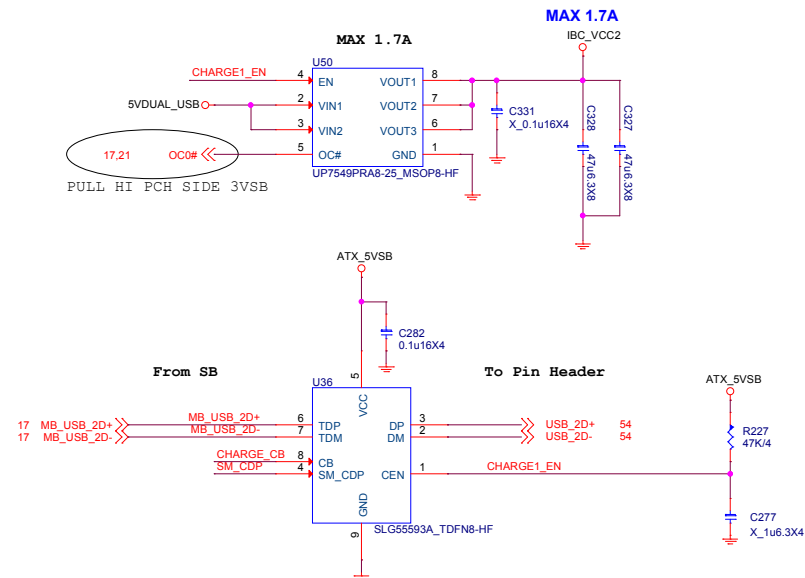
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging

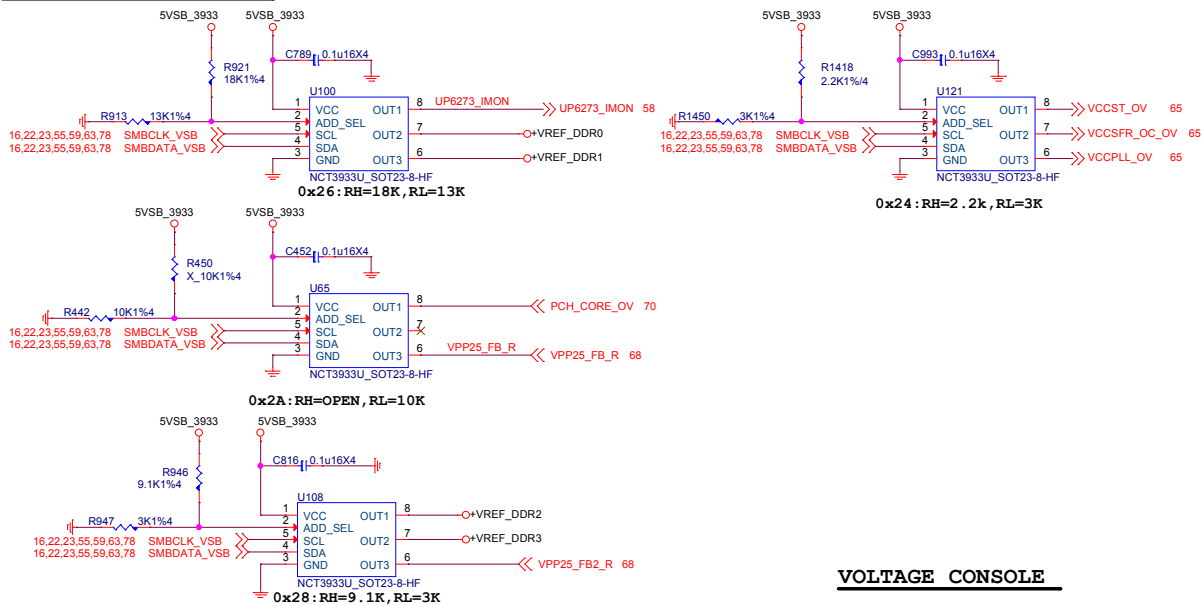


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Size	Document Description	Rev
Custom	USB CHARGE_SLG55593A	1.0
Date: Monday, May 15, 2017	Sheet 56 of 84	

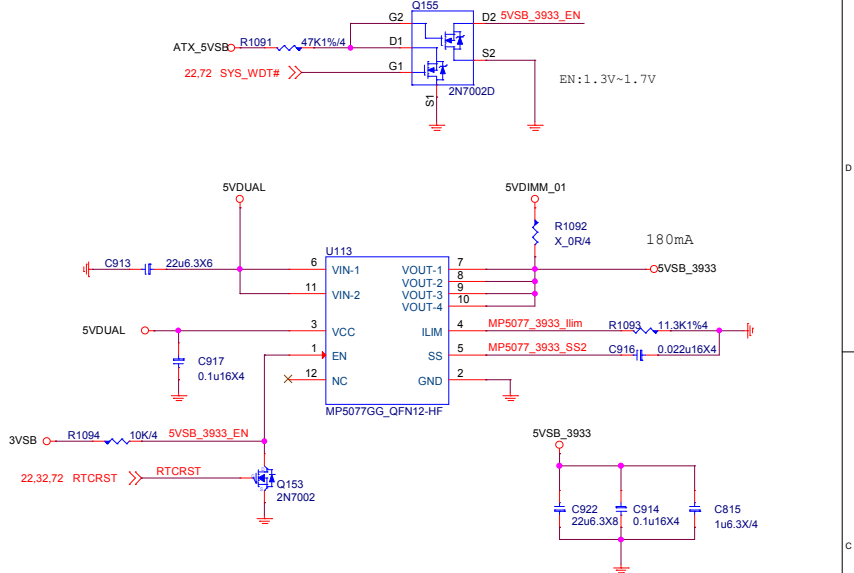
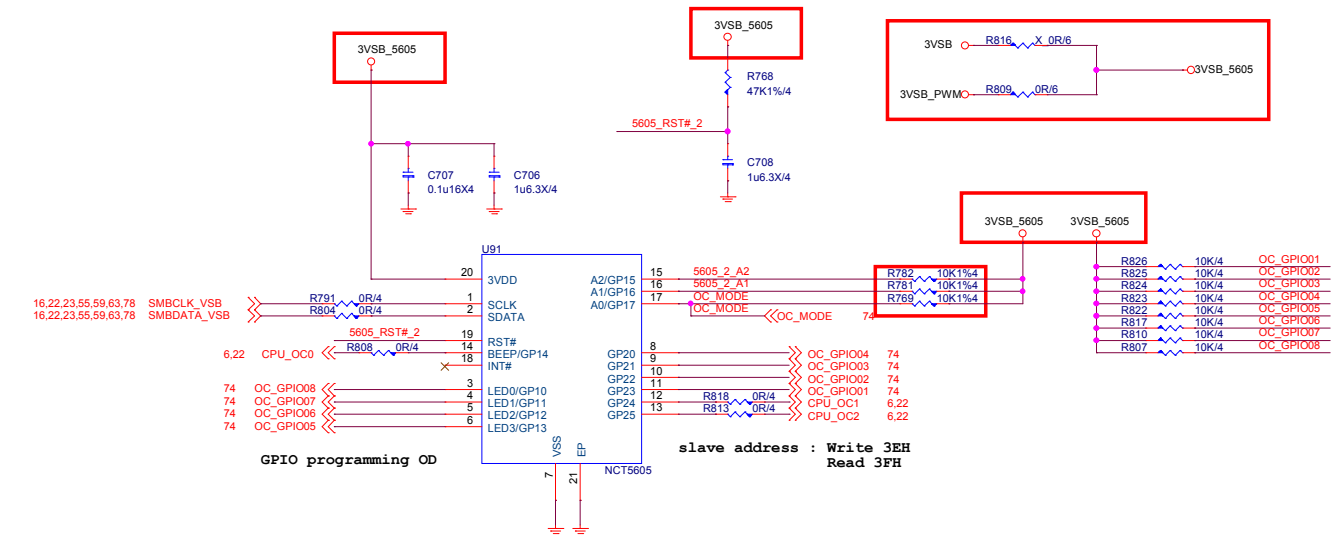
UPI VOLTAGE CONSOLE




VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

RSVD FOR OC





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Size Custom

Document Description

USB3.0 Connector

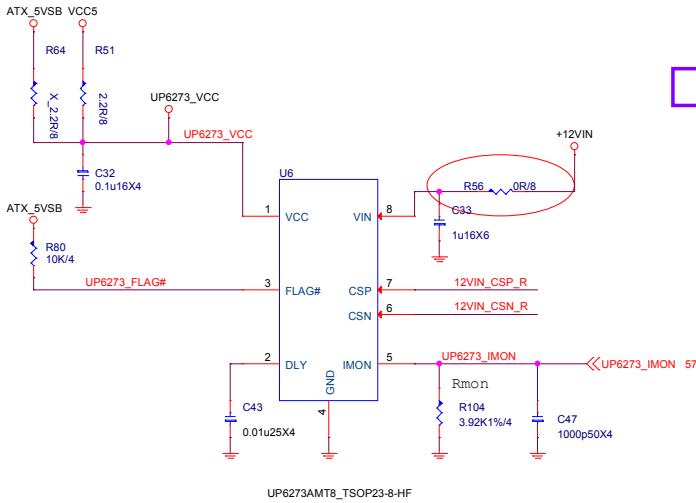
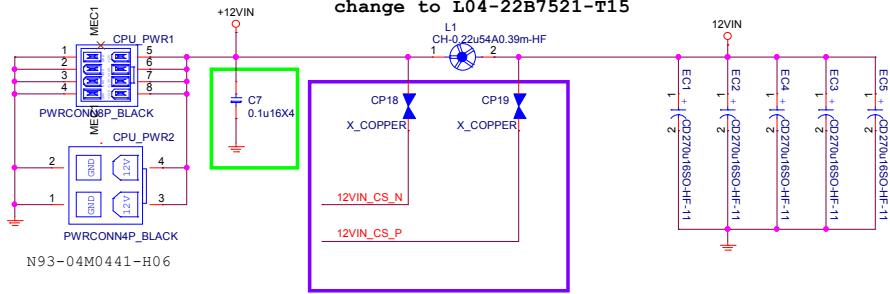
Date: Monday, May 15, 2017

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Rev 1.0

N93-08M0221-H06 Close Power Connector

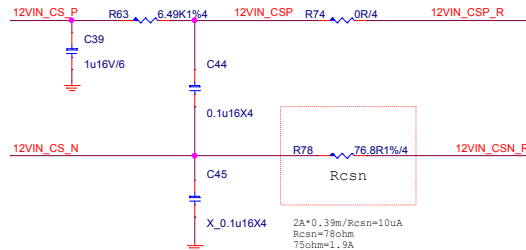
change to I04-22B7521-T15



$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$
 $V_{mon} = 1.2$
 can change OCP trigger level by Rcsn and Rmon

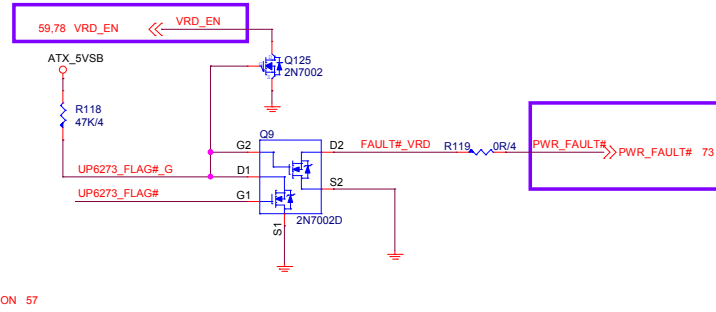
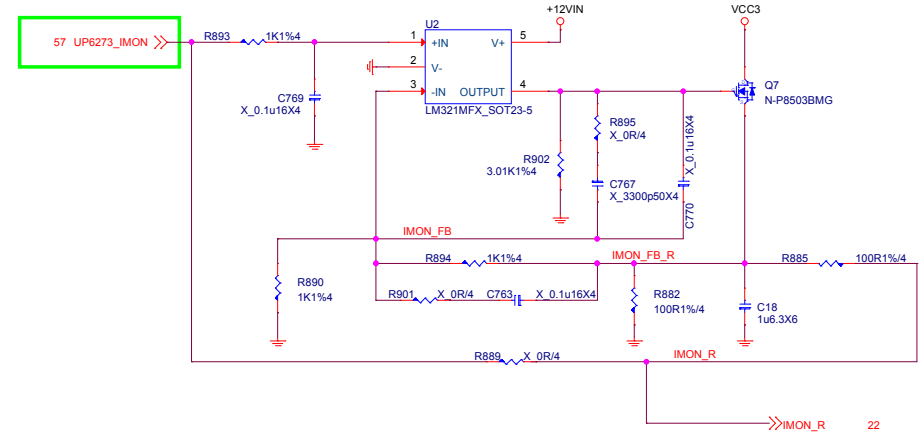
$R_{mon} = (1.2 \times 0.0768k) / (60 \times 0.39m)$
 $= 3.9k$

— 2A
 Rmon=1kOhm
 Rcsn=0.0768kOhm
 DCR=0.39mohm
 Vmon=1.2V
 Iocp=46.33484163A
 ocp=60A



2A*0.39m/Rcsn=10uA
 Rcsn=78ohm
 75ohm=1.9A

Near PWM IC



VRMPWRGD LEVEL SHIFT

Vcore: ICC Max 100A
LL: 1.0 mohm
OCP: 400A

VSA: ICC Max 15A
OCP: 40A

PROC_ID Sequence

PROC_ID	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X (IMVP8)

VSA VCC/VSS Sense IC Parameters

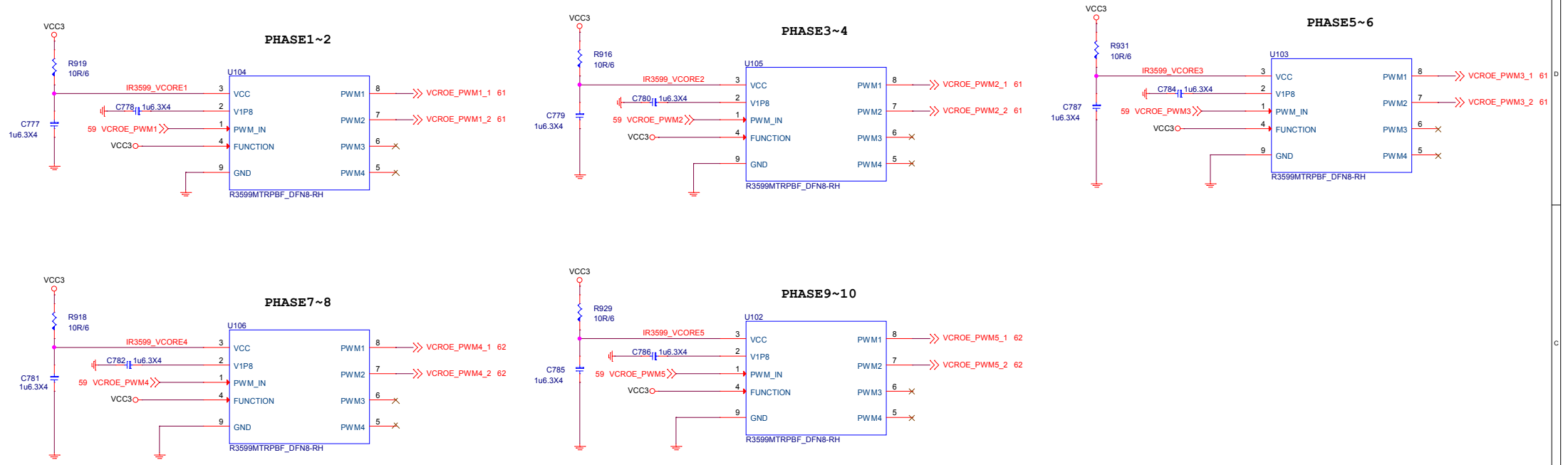
Temp	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

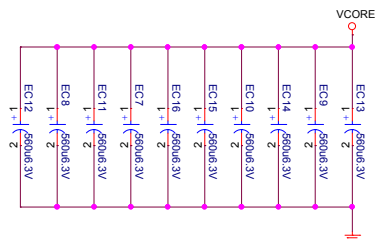
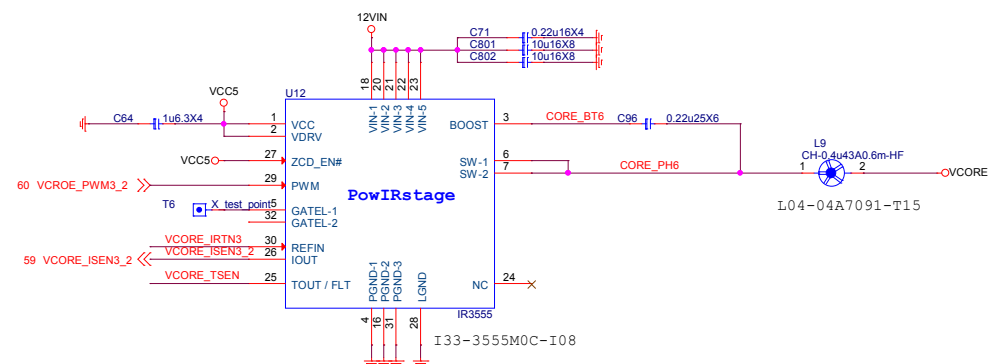
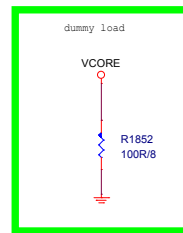
MICRO-STAR INT'L CO.,LTD

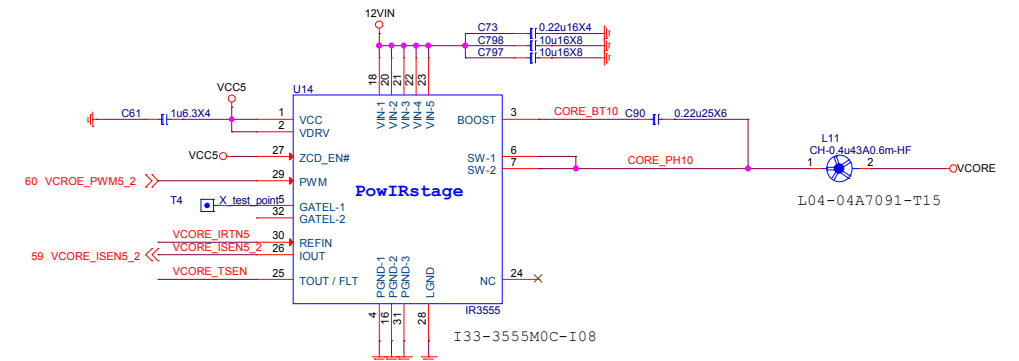
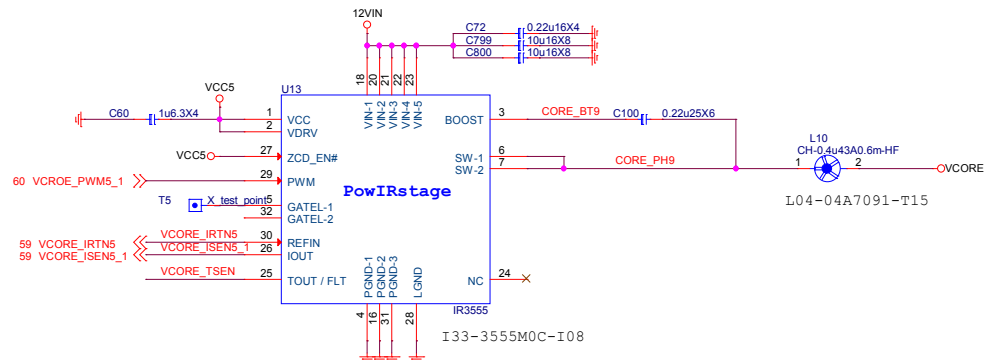
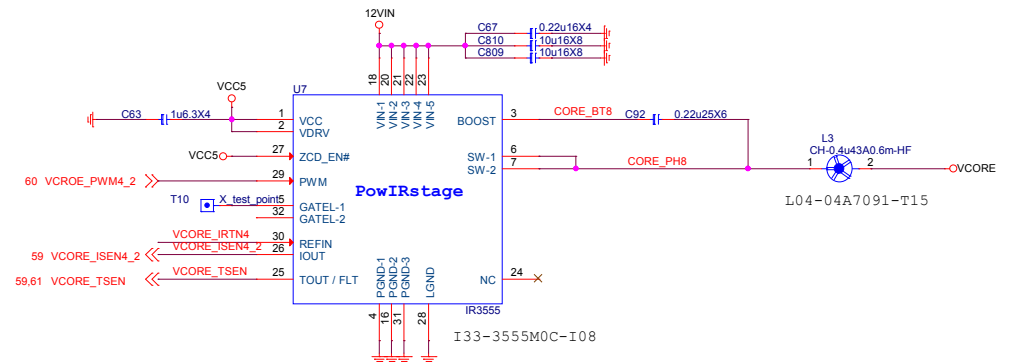
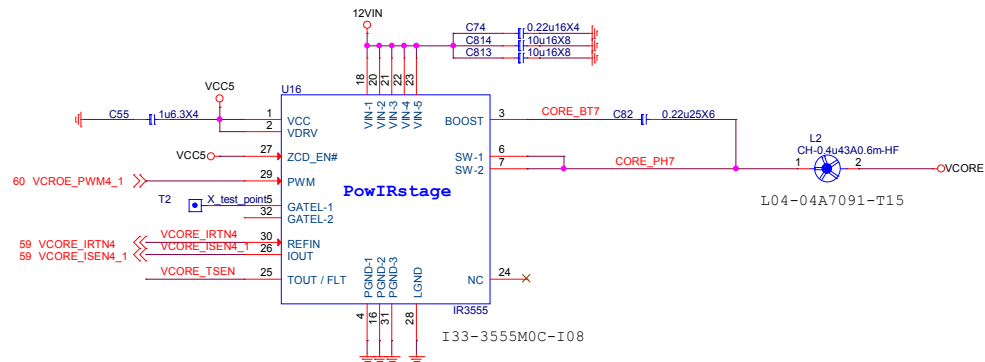
MS-7A95

Size: Custom
Document Description: CPU PWR-IR35201
Rev: 1.0
Date: Monday, May 15, 2017
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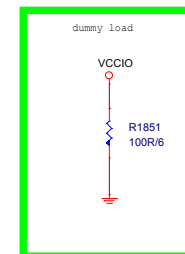
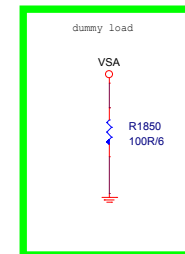
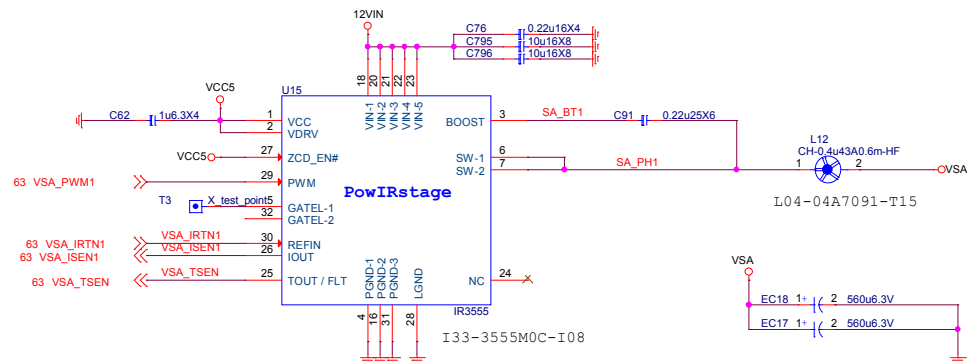
VCORE Double



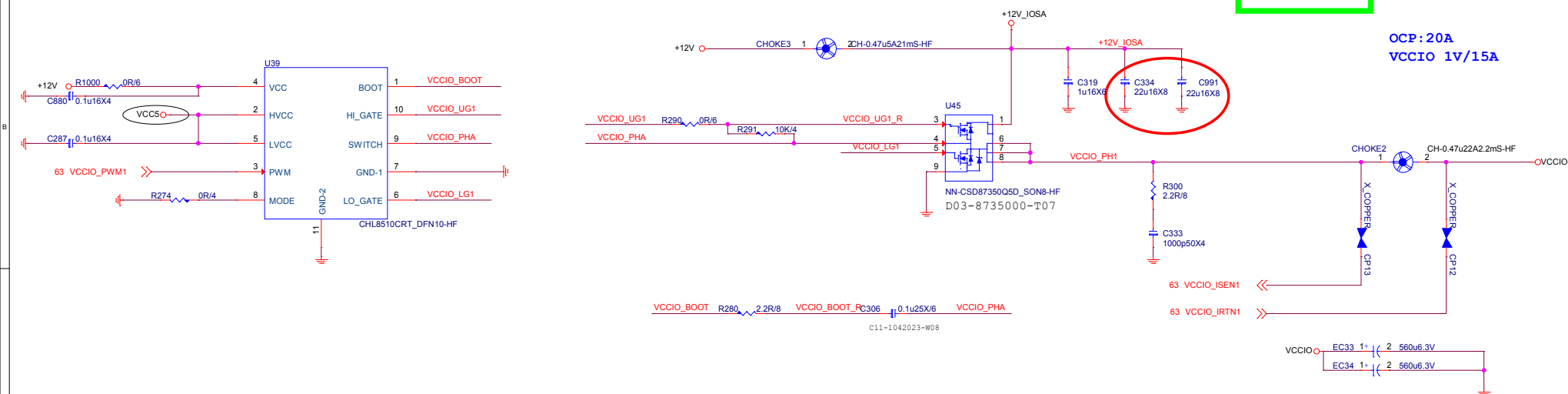




OCP:40A
VSA 0.5V-2.0V/ 15A



OCP:20A
VCCIO 1V/15A



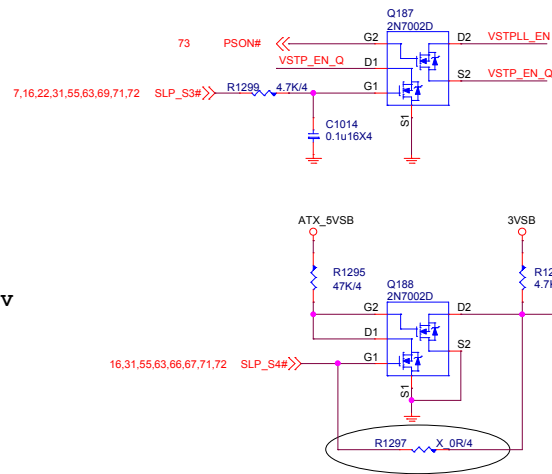
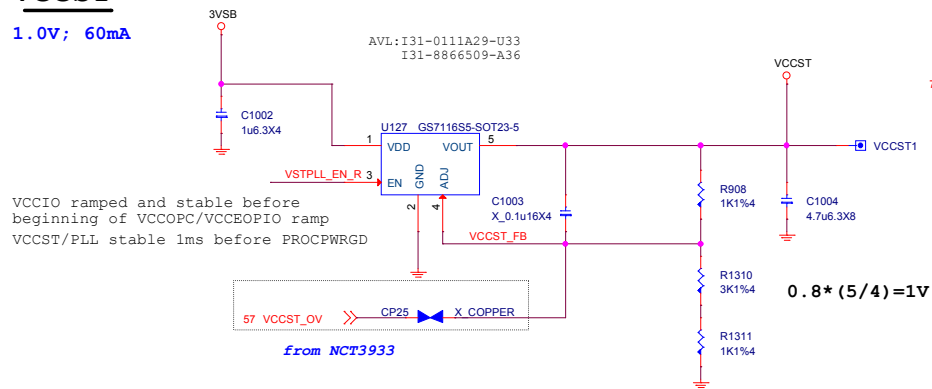
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Size	Document Description	Rev
Custom	VCCIO/VSA 1+1 PHASE	1.0
Date:	Monday, May 15, 2017	Sheet 64 of 84

VCCST

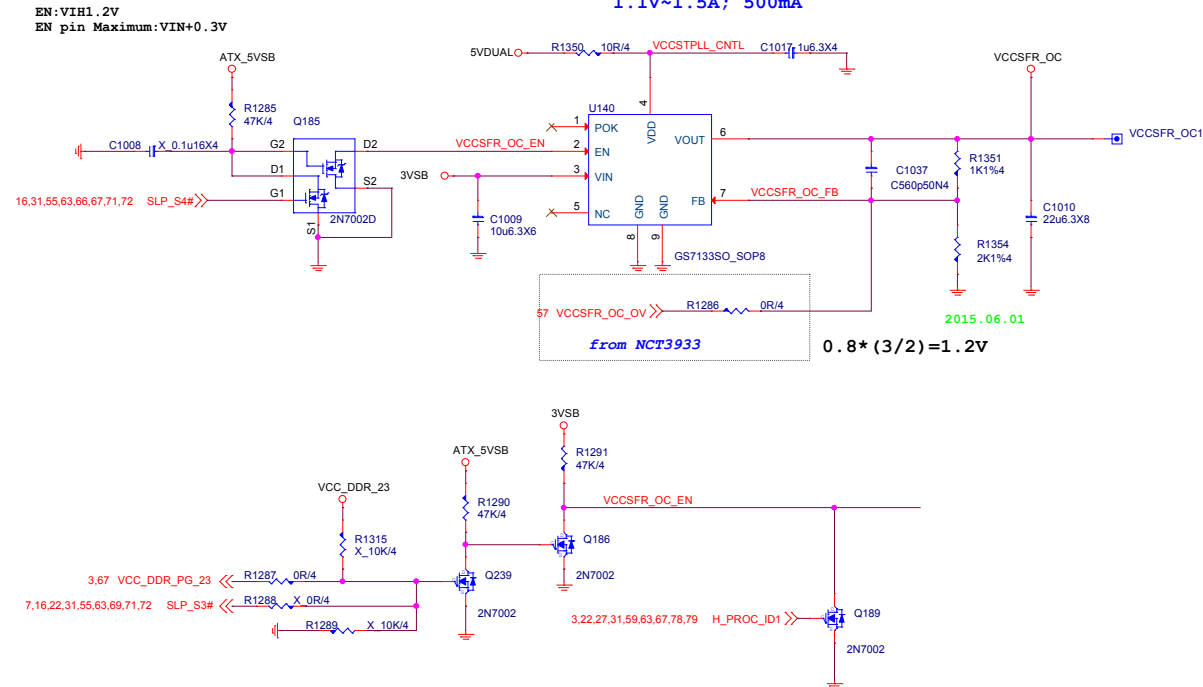
1.0V; 60mA



For non-OC system, configures +VCCSFR_OC as 1.2V

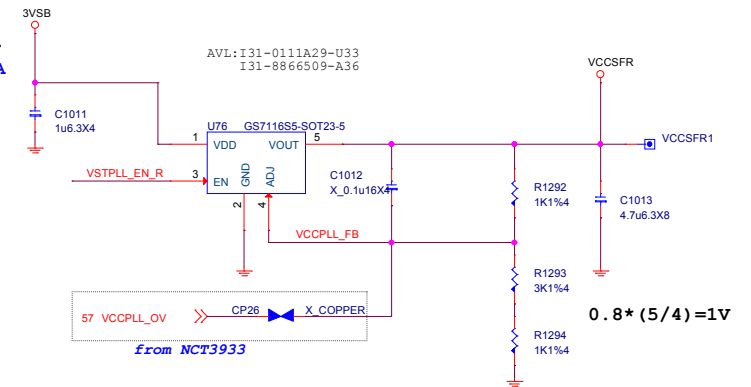
VCCSFR_OC

1.1V~1.5A; 500mA



VCCSFR

1.0V; 150mA

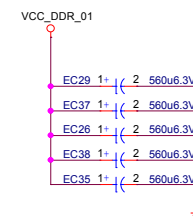
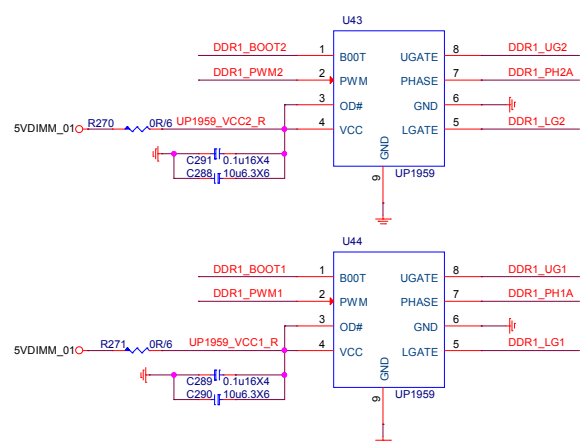
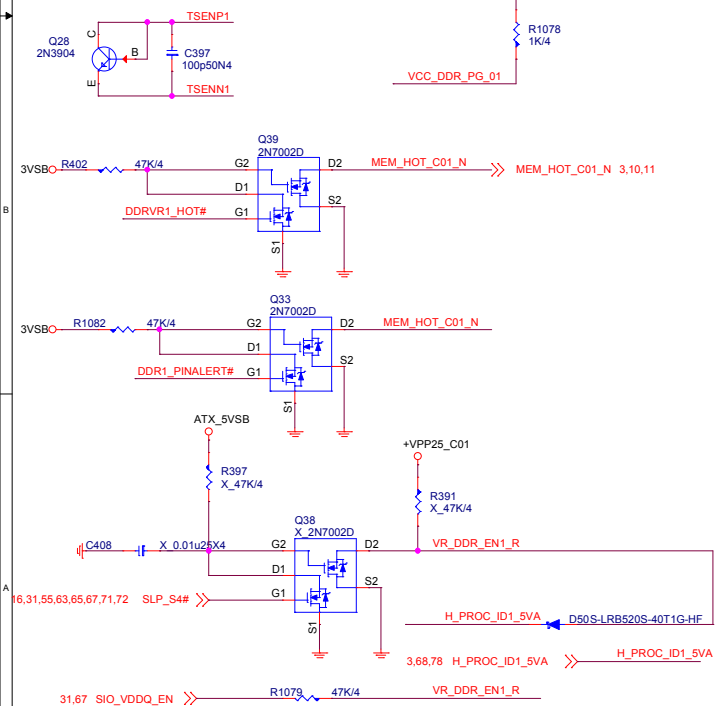
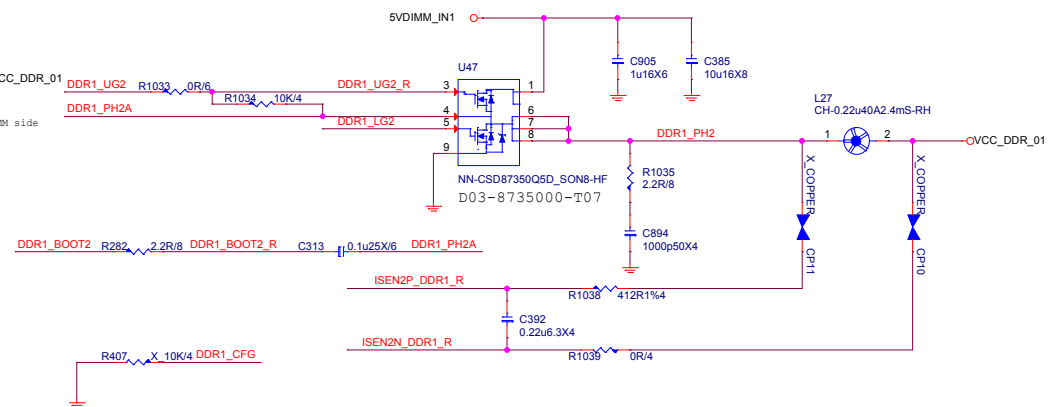
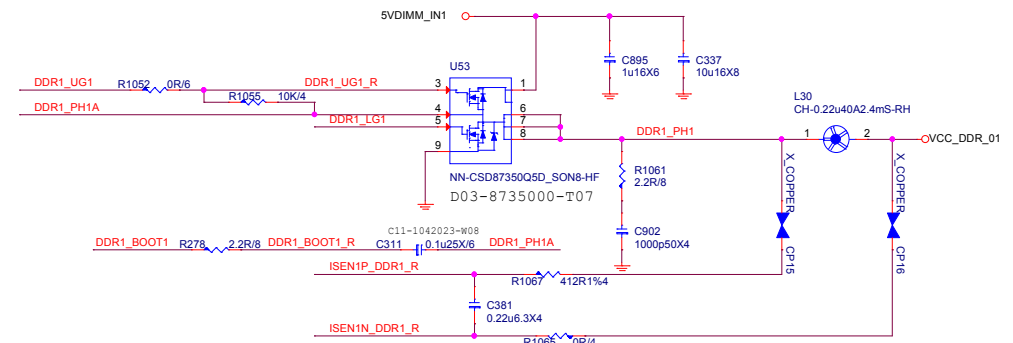


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MS-7A90

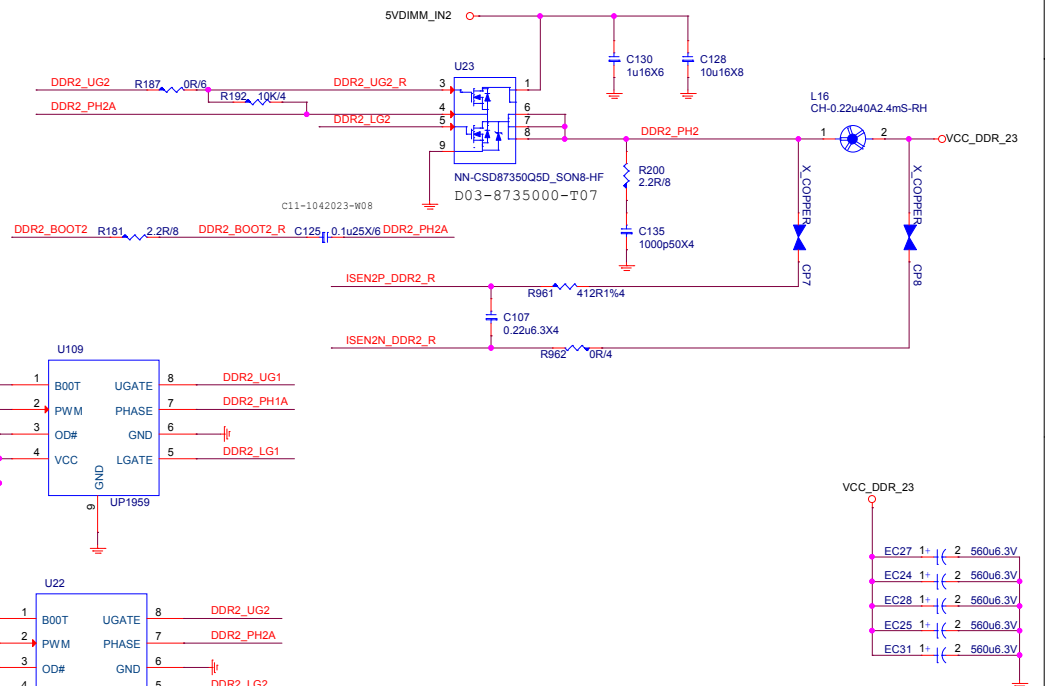
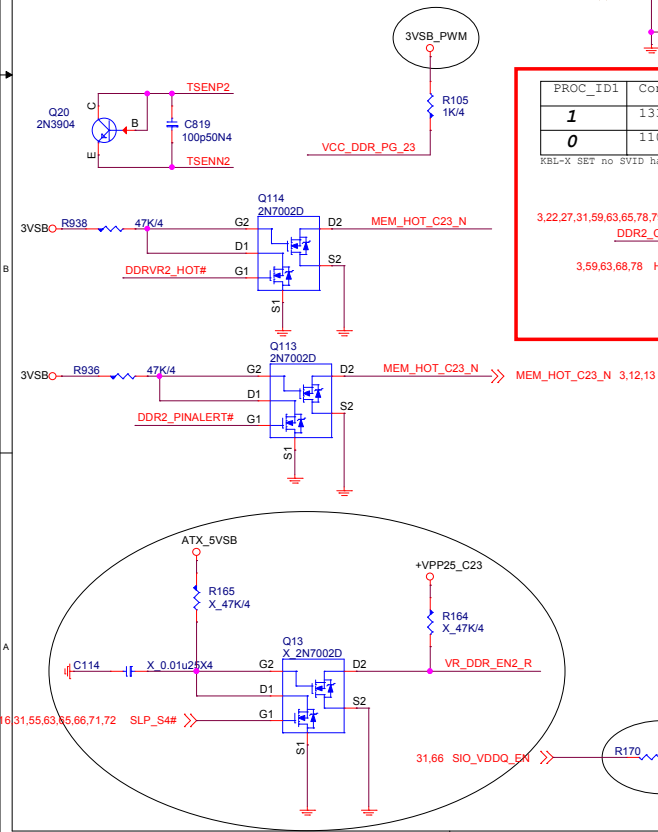
Size	Document Description	Rev
Custom	CPU VCCST/VCCSFR/VCCSFR_OC	10
Date: Monday, May 15, 2017	Sheet 65 of 84	

DDR4 1.2V nominal,
0.8V-2.5V Max, 44.14A / OCP 50A

**MS-7A95**

Size Custom	Document Description VR13_VCCDDR01 PV4201-2 phase	Rev 1.0
Date: Monday, May 15, 2017	Sheet 66 of 84	

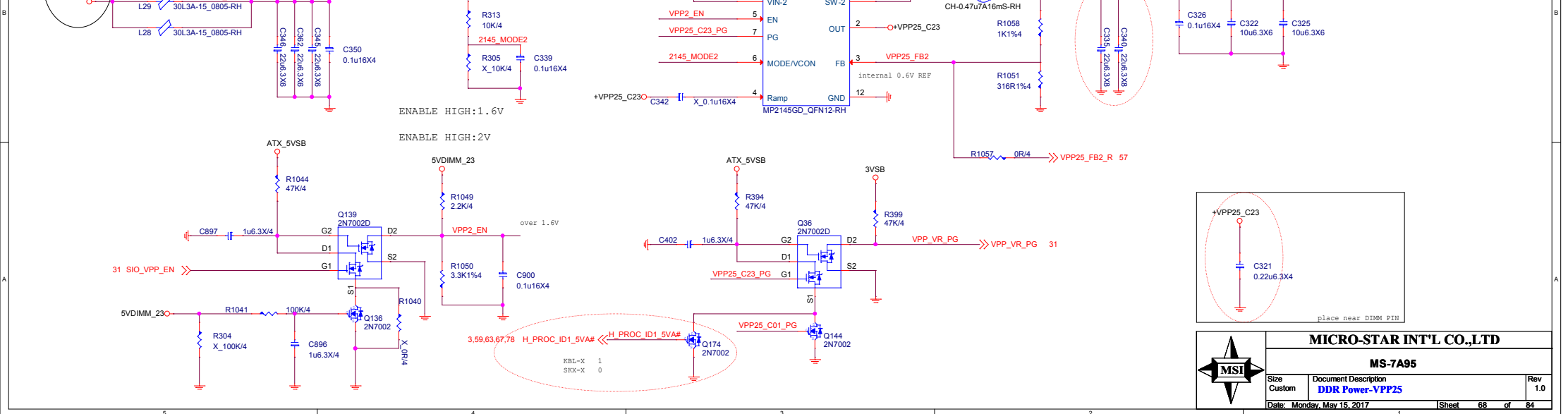
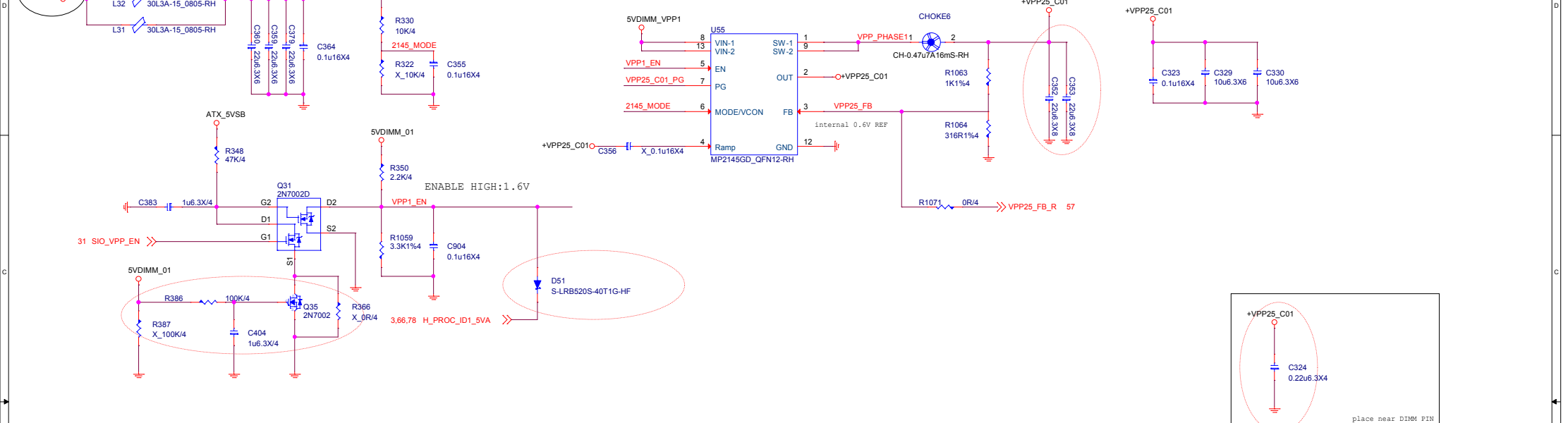
DDR4 1.2V nominal,
0.8V-2.5V Max, 44.14A / OCP 50A



MS-7A95

Size Custom	Document Description VR13_VCCDDR23 PV4201-2 phase	Rev 1.0
Date: Monday, May 15, 2017	Sheet 67 of 84	

5	4	3	2	1
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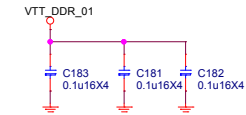
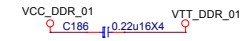
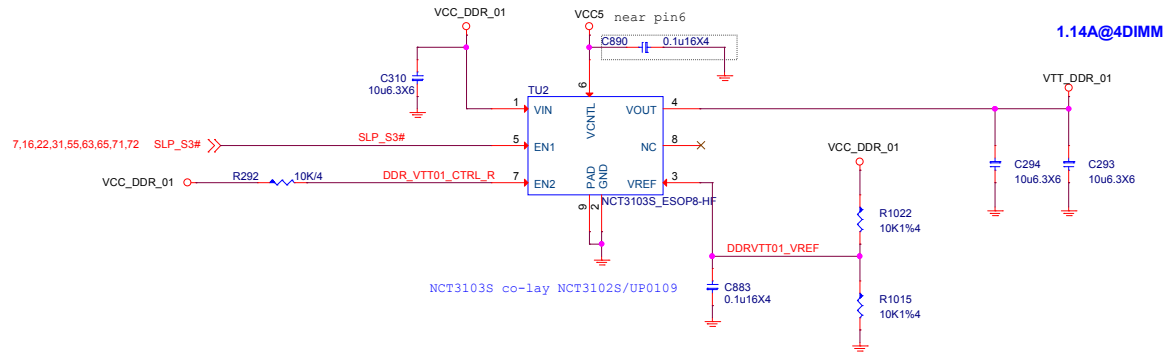
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Size Custom	Document Description DDR Power-VPP25	Rev 1.0
Date: Monday, May 15, 2017	Sheet 68 of 84	

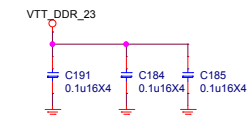
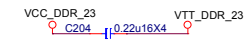
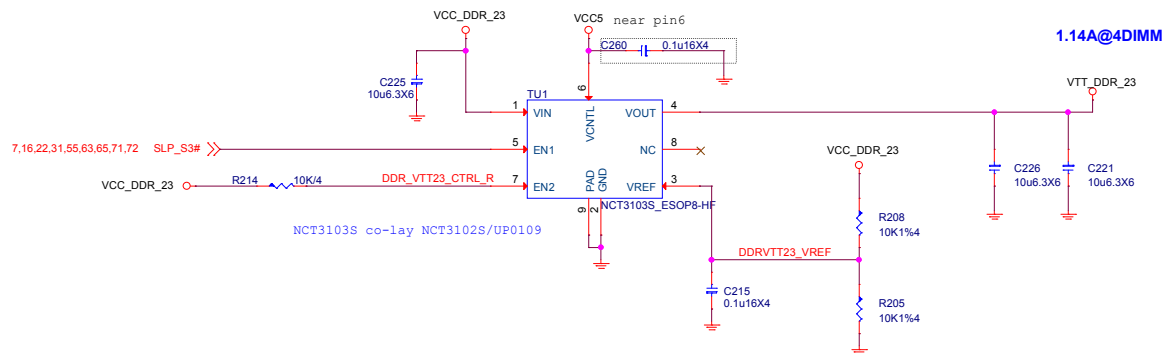
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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Size Custom	Document Description VTDDR	Rev 1.0
Date: Monday, May 15, 2017		
Sheet 69 of 84		

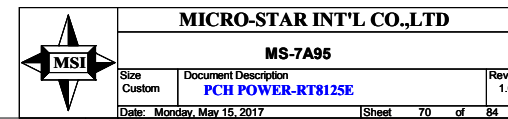

```
Rdson (low)
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm
```

$$\begin{aligned} V_{out} &= V_{ref} * (1 + R_{595}/R_{594}) \\ &= 0.8 * (1 + 1K/3.92K) \\ &= 0.8 * 1.2551 \\ &= 1.004V \end{aligned}$$

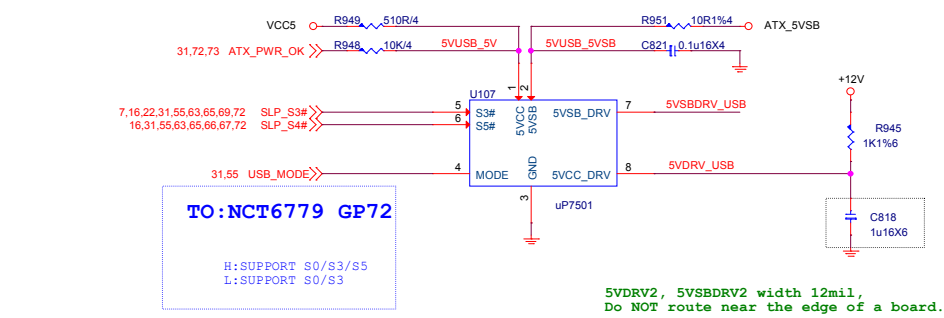
$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

$$= 0.8335 \mu H \quad (K = 30\%)$$

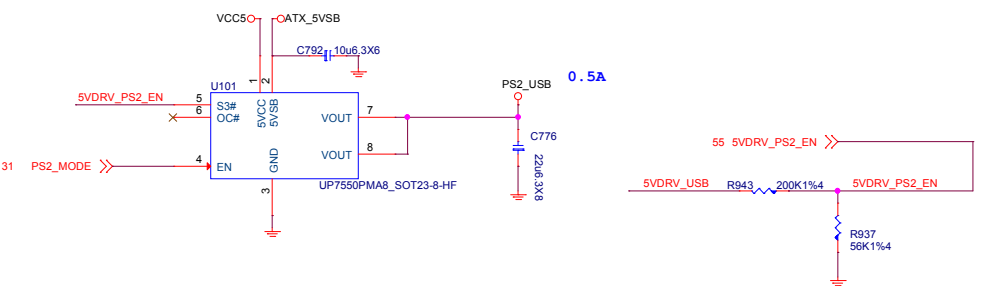
L04-01072H0-T15
L04-0107800-M26



USB POWER

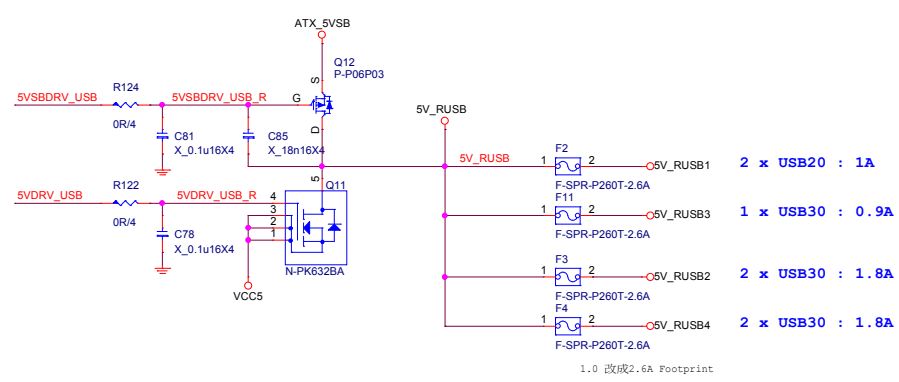


PS2 POWER

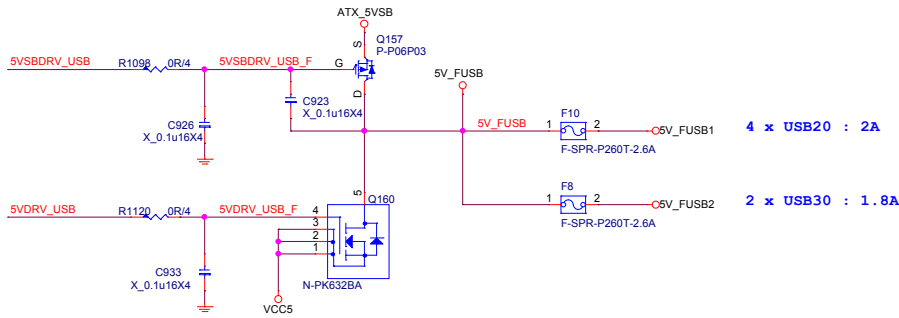


USB MODE

REAR USB PORT POWER



FRONT USB PORT POWER

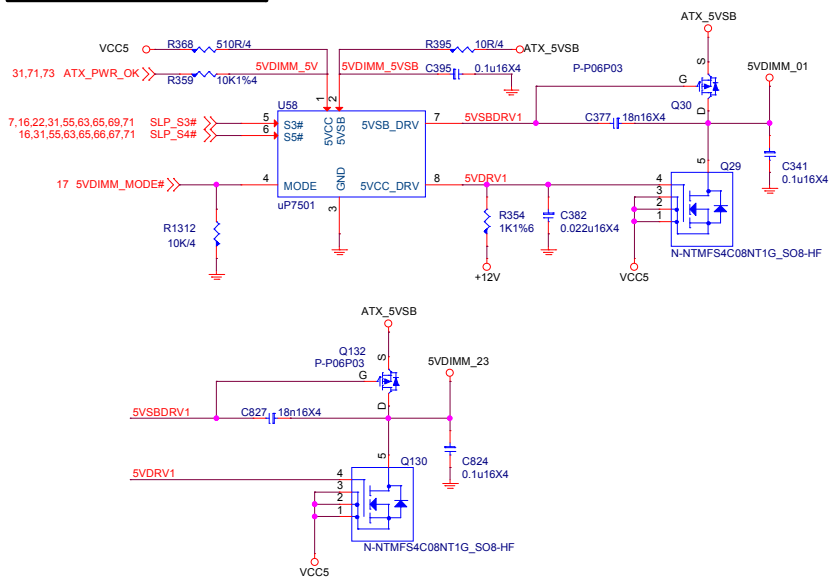


MICRO-STAR INT'L CO.,LTD

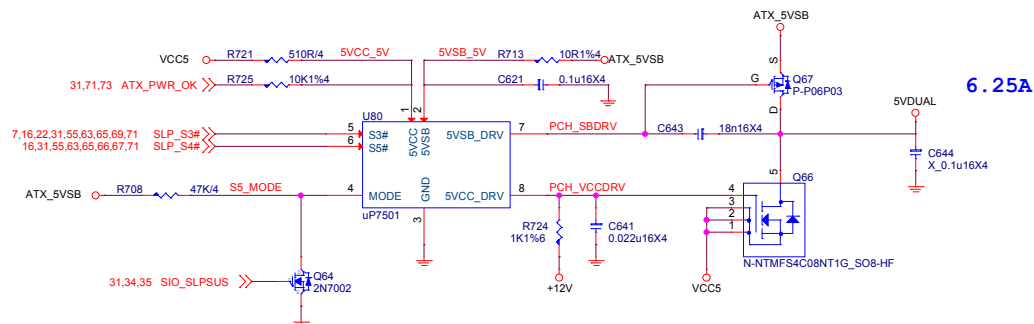
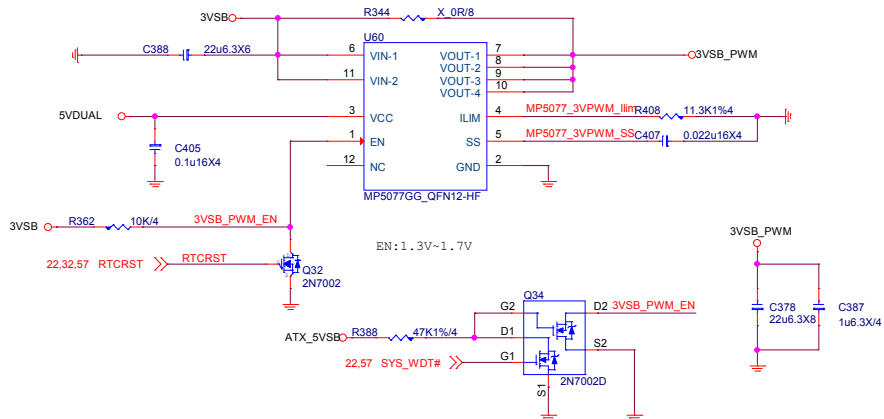
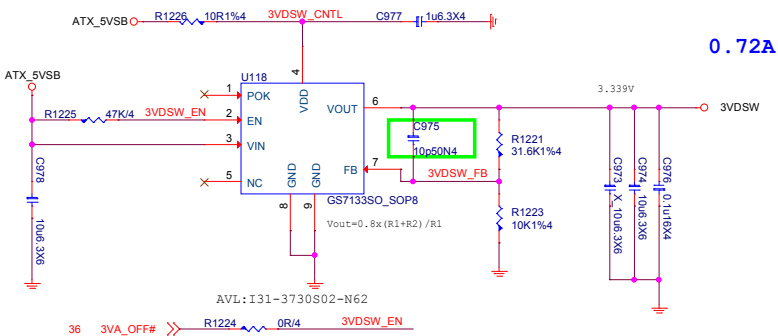
MS-7A95

Size Custom	Document Description USB Power	Rev 1.0
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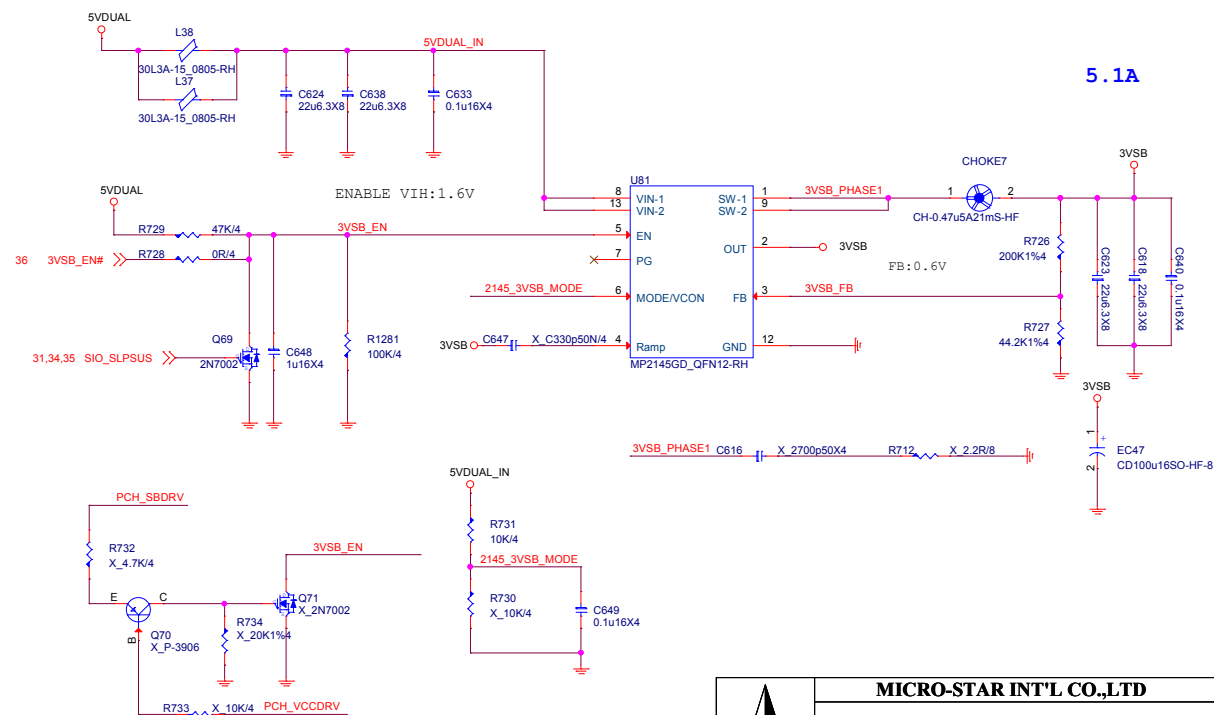
5VDIMM FOR DDR



3VDSW



3VSB *for OC & Gaming*



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop



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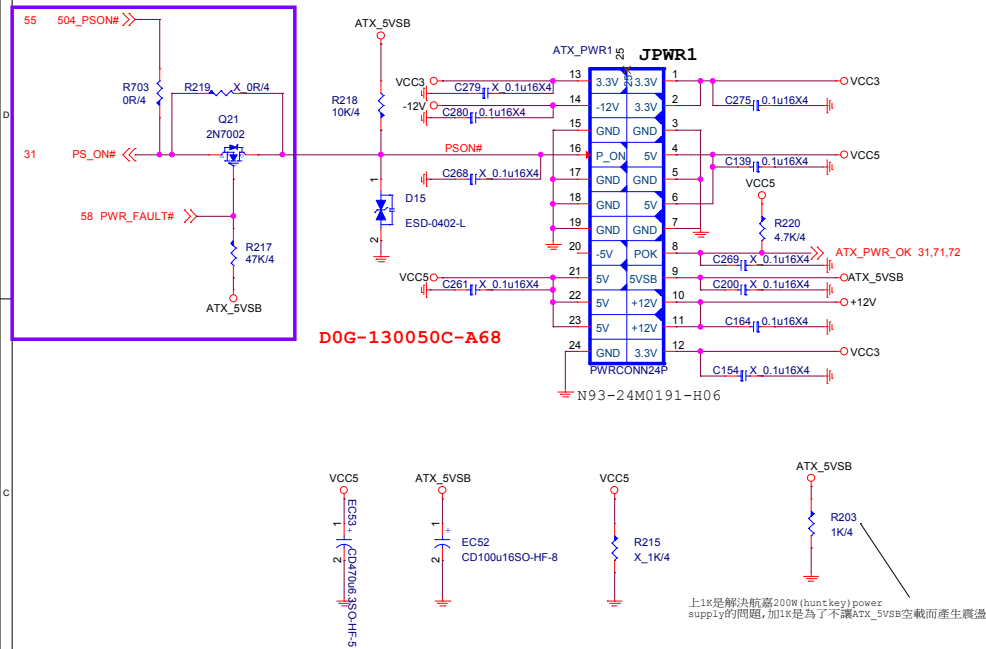
MS-7A95

Size	Document Description
Custom	ACPI-MPS

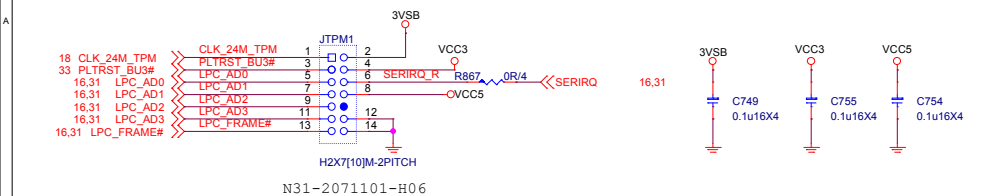
Rev

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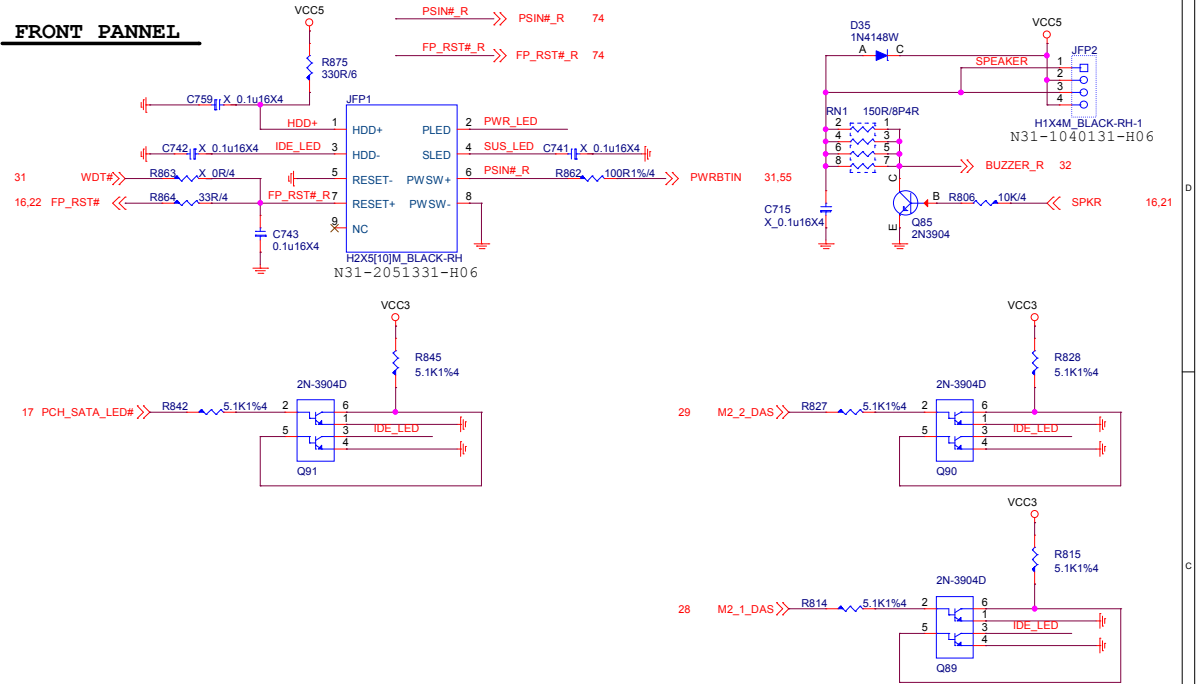
ATX POWER CONNECTOR



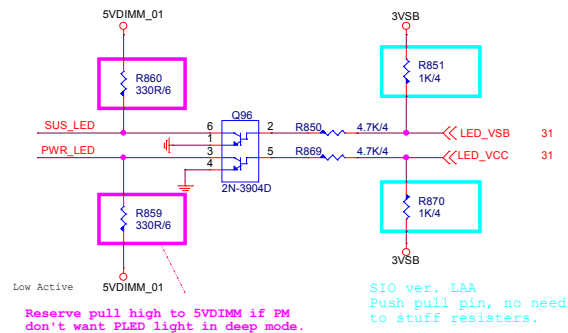
TPM Pin Header



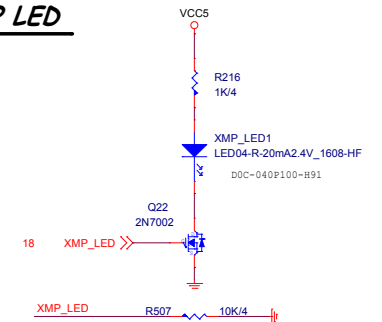
FRONT PANNEL



Front Panel LED

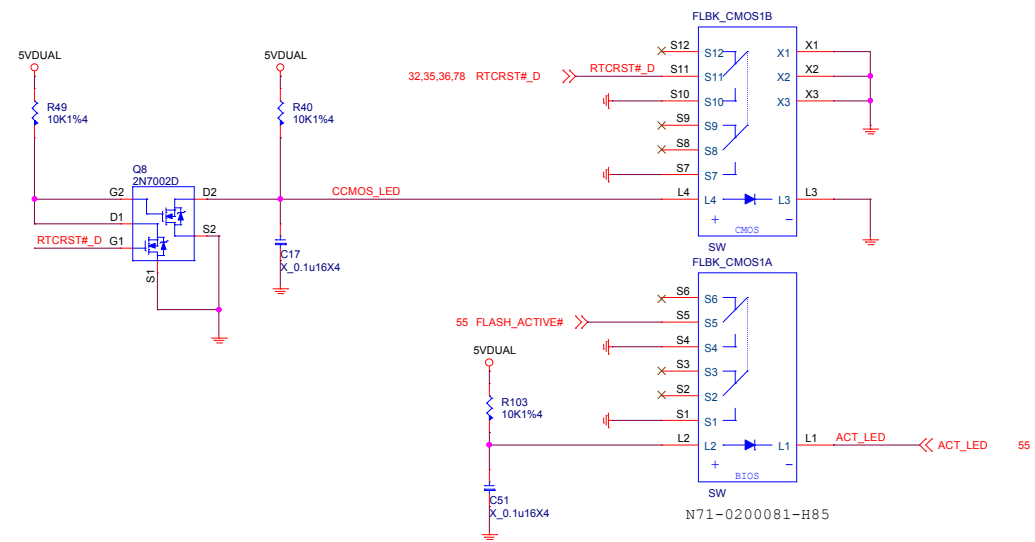
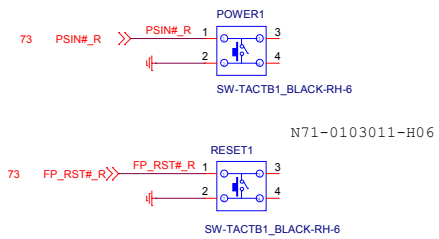


XMP LED

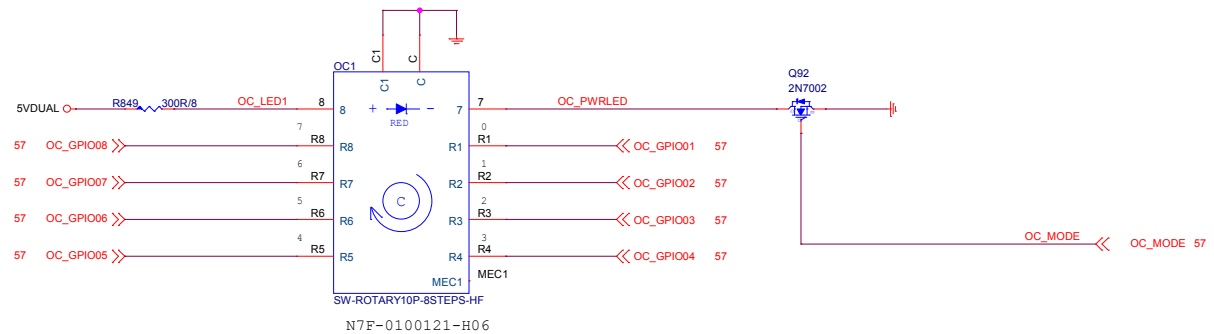


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MS-7A95		
Size Custom	Document Description ATX Connector/F_Panel	Rev 1.0
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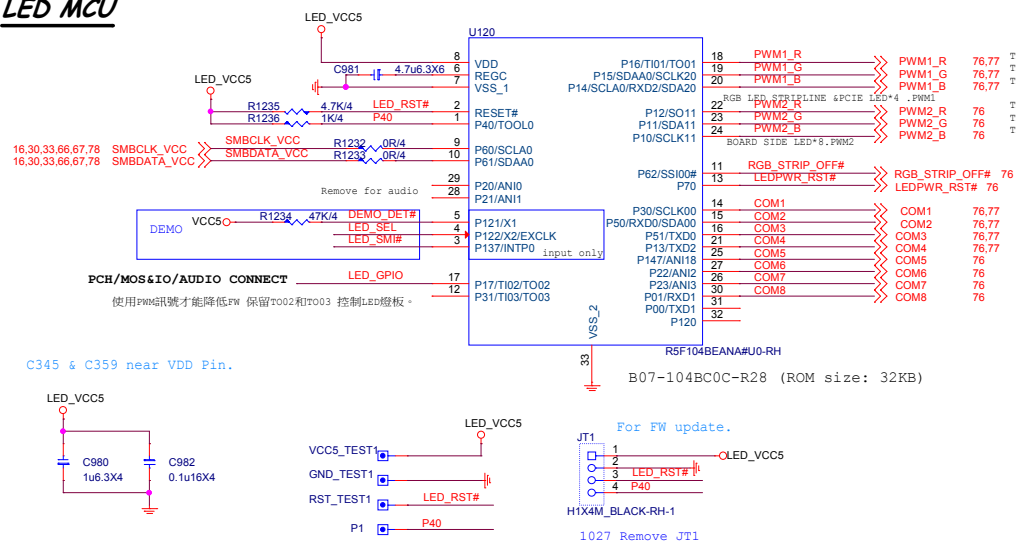
PWR/RST Botton



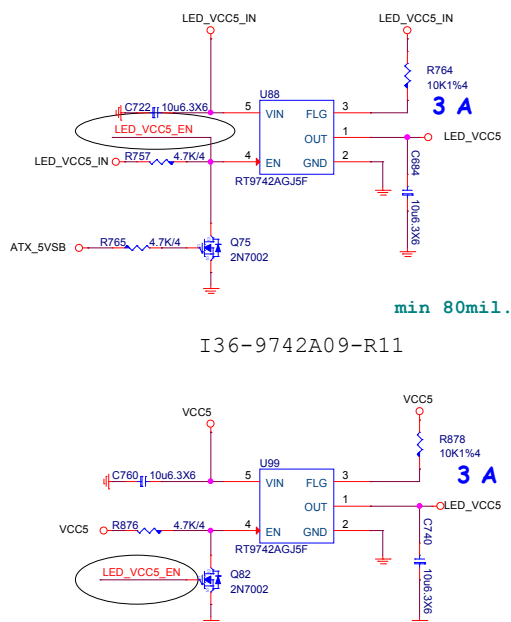
OC Genie



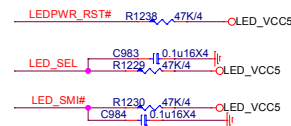
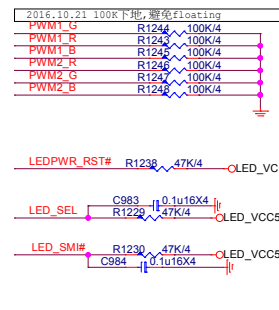
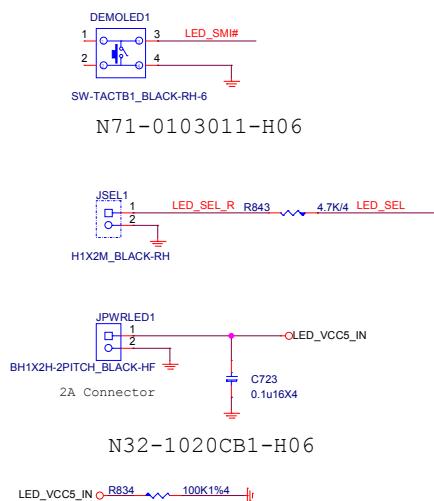
LED MCU



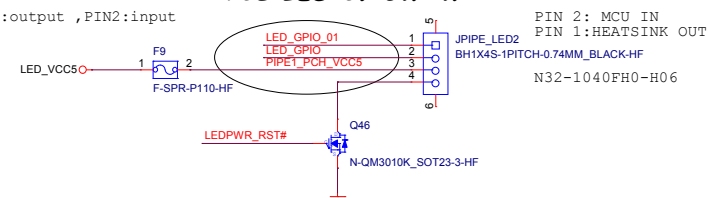
EXTERNAL POWER INPUT



LED Demo Button

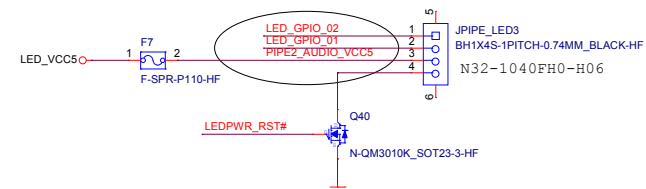


```
JPIPE:PIN1:output ,PIN2:input
```

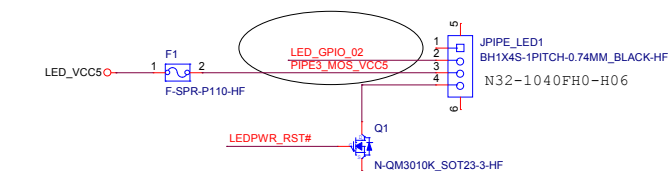


1 PCH HEATSINK LED
PCS LED*0.16W=W

2 AUDIO/IO Cover LED
PCS LED*0.16W=W



3 $\frac{\text{MOS HEATSINK LED}}{\text{PCS LED} * 0.16\text{W} = \text{W}}$



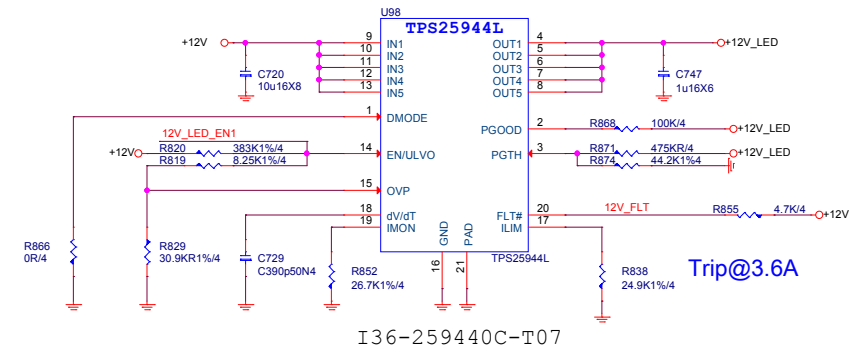
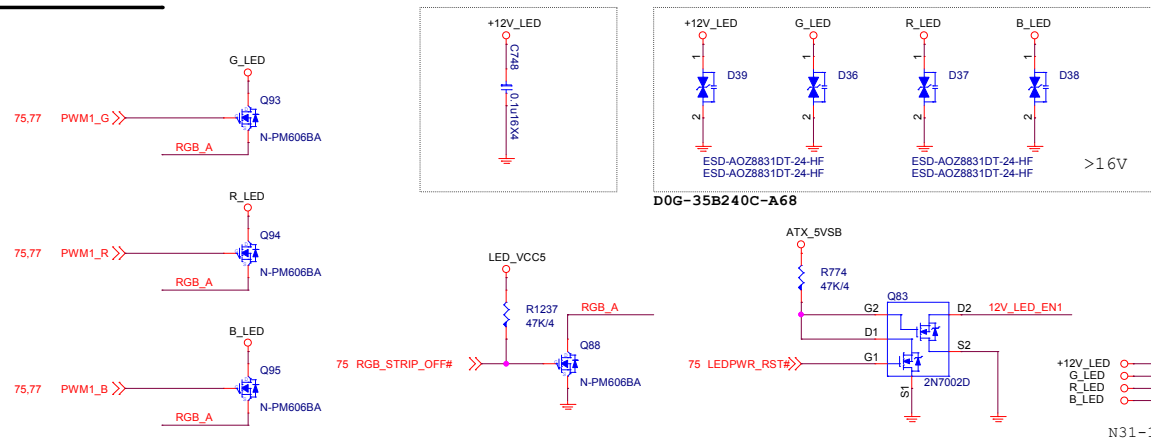
MICRO-STAR INT'L CO.,LTD

MS-7A95

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LED STRIPLINE

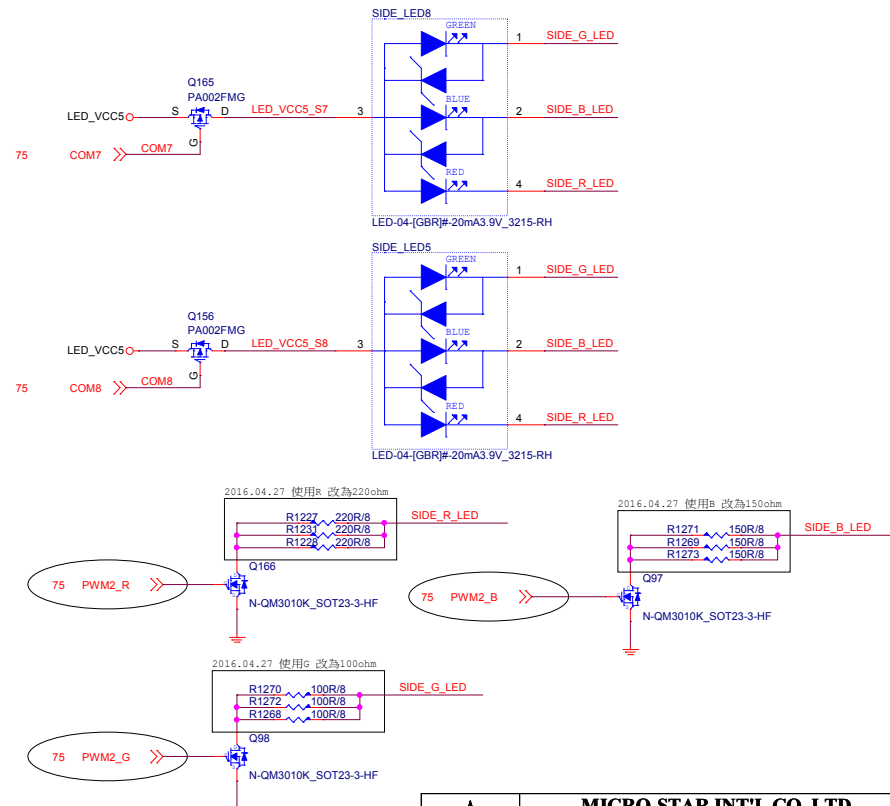
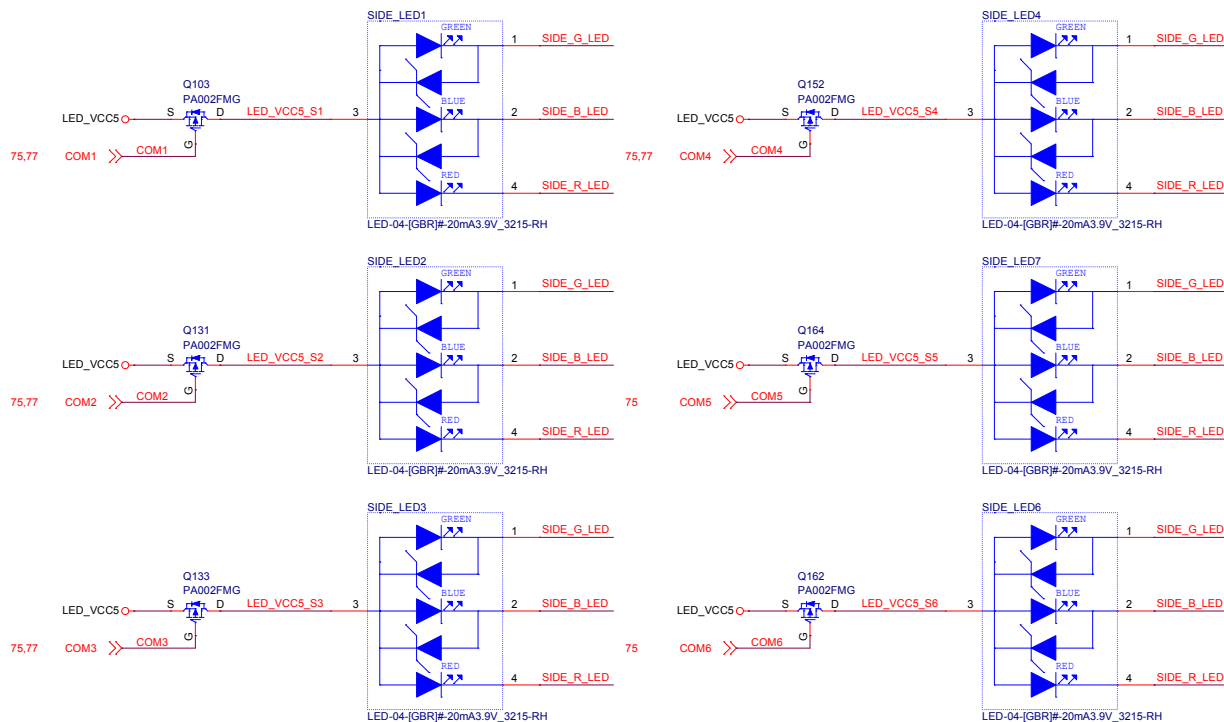
2016.07.06 only reserve now
2016.08.02 Add +12V_LED 0.1uF
2016.08.02 stuff ESD



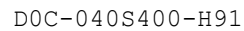
外接LED 燈條 (RGB)
---- PCB 文字面 (JLED1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺 (待7A20驗證)

BOARD SIDE LED *8

DOC-040R700-H91
Forward Current 20mA
Pulse Forward Current 30-60mA



D0C-040P100-H91/D0C-040S500-E07



MICRO-STAR INT'L CO.,LTD

MS-7A95

	Size
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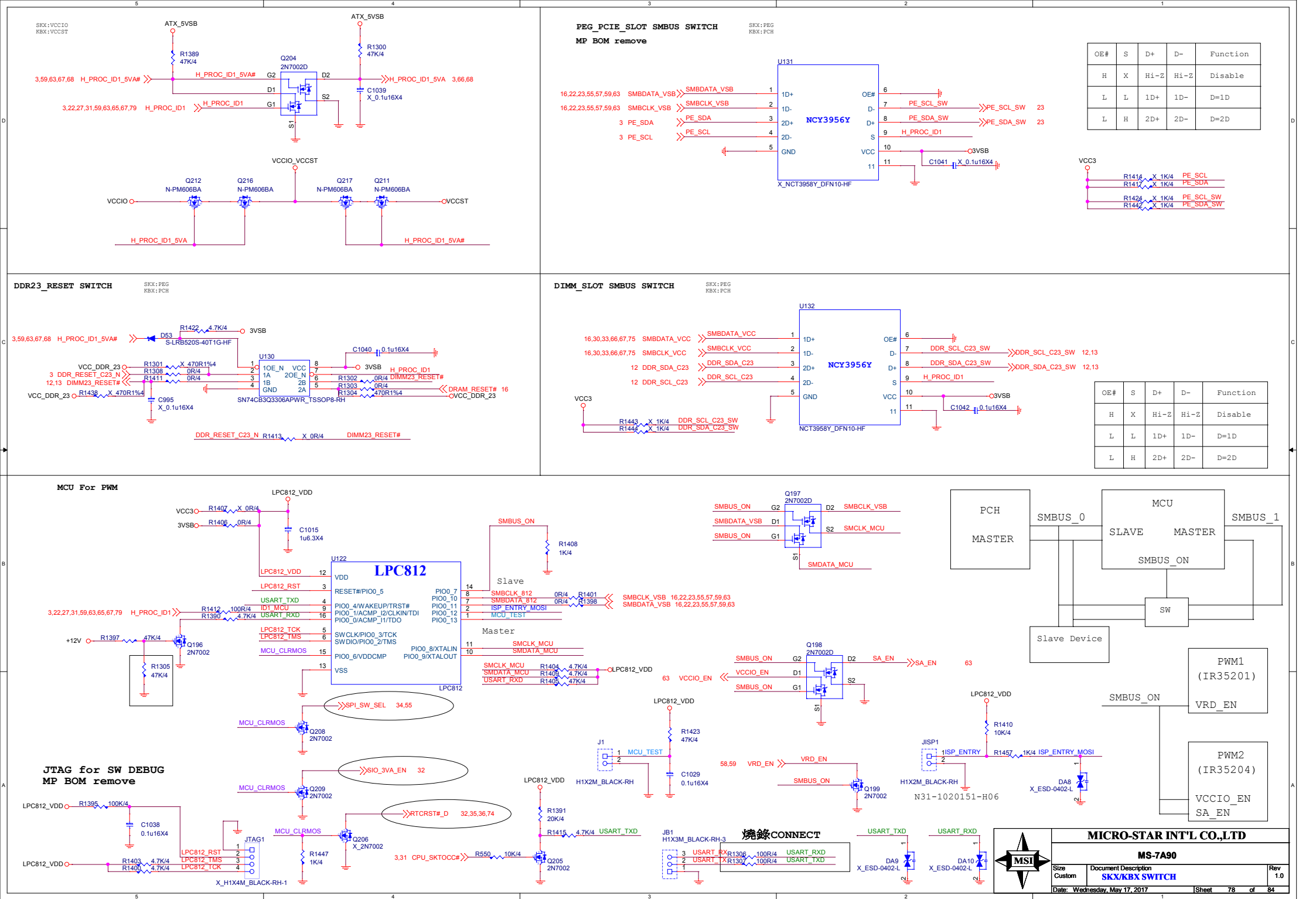
Document Description

DIMM LED

Rev
1.0

Date: Monday, May 15, 2017

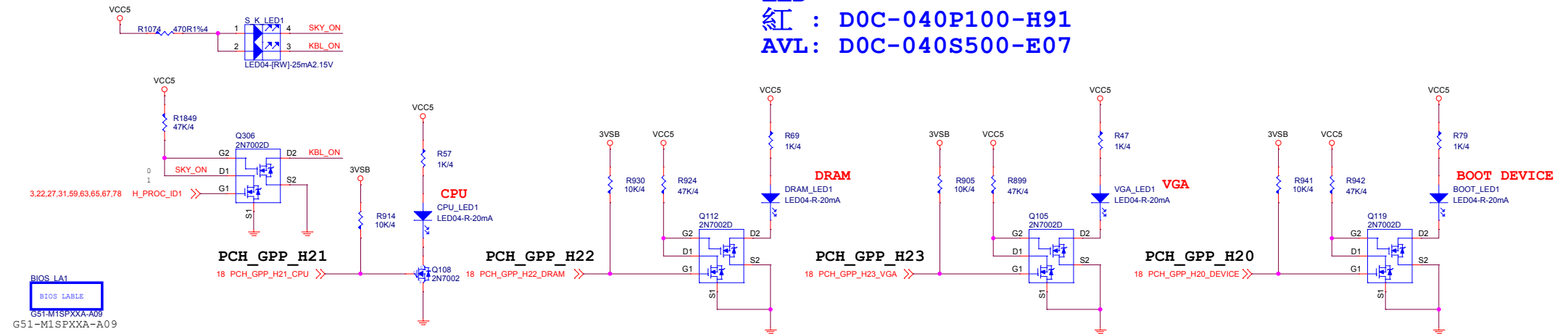
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LED

紅 : D0C-040P100-H91

AVL: D0C-040S500-E07

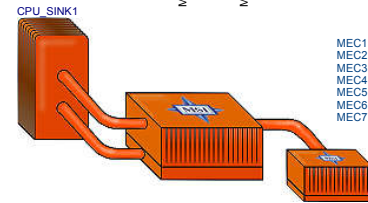
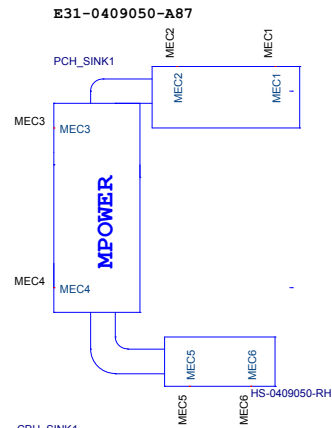


GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

開機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED減掉。
5. 因此最後正常順利開機後，四個LED燈都是減掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

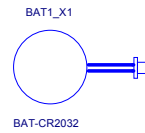
BIOS LA1
G51-M1SPXXA-A09
SLI1
Label
Y01-RNVIDIL-000
SSE1
Label
Y02-MA00101-SSE
XSPLT1
Label
Y02-MA00401-XSP
NAHIMIC1
Label
Y02-MU00100-NAH
CFOS1
Label
Y02-MU00170-CFO
MKT1
Label
G51-M1SPL72-Q13



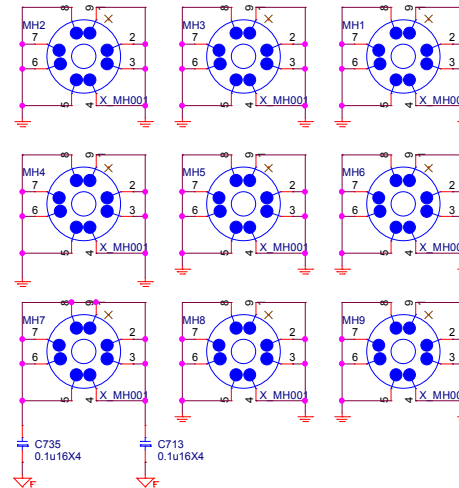
HS-0504900-A87

CPU 鐵座
CPU_ILM1
E21-7A95020-I06
AVL: E21-7A95-050-F02

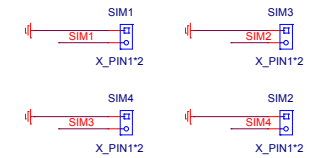
CHOKE COVER
X1
X2
X_CHOKE_COVER



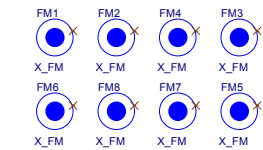
Mounting Holes



Simulation



Optical Fiducial Marks-120



VCCORE VCCIN1
VSA VCCSA1
VCCIO VCCIO1
VCC_DDR_01 VCC_DDR_01
VCC_DDR_23 VCC_DDR_23
VTT_DDR_23 VTT_DDR_23
VTT_DDR_01 VTT_DDR_01
5VDUAL 5VDUAL1
5VDIMM_01 5VDIMM_01
5VDIMM_23 5VDIMM_23
3VSB 3VSB1
VBAT VBAT1
+VPP25_C23 VPP25_C23
+VPP25_C01 VPP25_C01